International Research Journal in Advanced Engineering and Technology (IRJAET)

ISSN (Print) : 2454-4744 | ISSN (Online) : 2454-4752 (www.irjaet.com)

Vol. 1, Issue 1, pp.31-35, June, 2015

RESEARCH ARTICLE

DISCRETE WAVELET TRANSFORM FOR IMAGE COMPRESSION AND RECONSTRUCTION VIA VLSI

D. Sobya

Department of Electronics and Communication Engineering, Research scholar: Sathyabama University
e-mail: sobyadevaraj@gmail.com

ARTICLE INFO

Article History:

Received 25th, May, 2015
Received in revised form 15th, June, 2015
Accepted 29th,June, 2015
Published online 30th, June, 2015

Key words:

Image
Discrete Wavelet Transform
FIR filter
FPGA

ABSTRACT

Image compression is one of the majority assure subject in image processing. The demand for higher quality images transmitted quickly over the internet has led to a strong need to develop better algorithms for the filtering and coding of such images. In this article the Discrete Wavelet Transform (DWT) is to be used for the compression and reconstruction of images together with an efficient coding scheme. The use of wavelets implies the use of sub band coding in which the image is iteratively decomposed into high- and low frequency bands. Thus there is a need for filter pairs at both the analysis and synthesis stages. Introduction of the DWT to illustrate its link with filters and filter banks and also to exemplify how it may be used as part of an image compressing algorithm had been carried out in this research.

I. INTRODUCTION

Day by day a huge amount of information is stored, processed and transmitted through IT field. Because much of this information is graphical or pictorial in nature, the storage and communications requirements are immense. The underlying basis of the reduction process is the removal of redundant wavelet transform. A wavelet based method is proposed for the actual signal processing, which performs signal decomposition more efficiently than the traditional Fast Fourier Transform (FFT) technique. Wavelets are a category of bases that are generated by the dilation and translation of a mother wavelet function. Since the wavelet analysis method can effectively localize a signal in both time and frequency domains it finds wide applications in signal processing. The transform is one of three major building blocks in waveform image compression systems, where quantization and coding are the two other blocks. It has been stated in the literature by many researchers that choice of decomposition transformation is a critical issue, which affects the performances of the image compression system. In many signal processing applications including compression, denoising and enhancement, performing the One-

Dimensional Discrete Wavelet Transform (1D DWT) is a good start. It has also been noted previously that the energy of the wavelet scales along with the time series skewness and kurtosis (i.e., the 3rd and 4th moments of the value distribution) form a suitable feature vector for signal classification. For example, the energies of the 1D wavelet scales 2 to 9 could be used, along with the skewness and kurtosis to build a feature vector with 10 input components. Skewness is sensitive to the unipolarity of the signal. Kurtosis is a measure of the tail of the distribution. The computation of 1D DWT is complex and it is occasionally difficult to meet the requirements of real time operation and speed. It is also of interest to have an implementation solution that allows flexibility in customizing the wavelet transform with regard to the filters being used and the structure of the wavelet decomposition tree. In this paper, we propose a novel and efficient Field Programmable Gate Array (FPGA) architecture for the implementation of 1D DWT. The architecture has been coded in VHSIC Hardware Description Language (VHDL), and has then been verified successfully by simulations on the Quartus II platform.

II. LITERATURE REVIEW

The VLSI architectures proposed in [1-3] for hardware implementations of DWT are mainly convolution-based. In the conventional convolution method of DWT, a pair of Finite Impulse Response filters (FIR) is applied in parallel to derive high pass and low-pass filter coefficients. The architecture is developed for lossy compression, which is based on the lifting algorithm of Daubechies filters and ensures that the image pixel values given to the DWT process which gives the high pass and low pass coefficients of the input image [4]. Wavelet transform has gained widespread acceptance in image compression research in particular. Wang [5] presented a folded architecture for lifting-based wavelet filters to compute the wavelet butterflies in different groups simultaneously at each decomposition level. Wei Zhang et al proposed the architecture in which it only requires minimum registers between the row and column filters as the transposing buffer, and a higher efficiency is achieved [6&9]. Usha Bhanu.N [7] analyzed the existing Lifting based 1-dimensional and 2-dimensional Discrete Wavelet Transform based on the hardware complexities and computational time for the different architectures using Lifting schemes. The architectures represented vary from direct mapped, folded, recursive to multilevel folded architectures. Dillen presented a combined architecture for the (5, 3) and (9, 7) transforms with minimum area [8]. FPGA is implemented in SPARTAN 3E. Power and Area analysis is done using Xilinx ISE and low power is achieved by Adithya [10]. Murali [11] reports the use of FPGA for implementation of neural network and DWT architecture, the design operates are 127 MHz and consumes 0.45 mW on Virtex-5 FPGAs. The DWT, based on timescale representation, provides efficient multi-resolution sub-band decomposition of signals. It has become a powerful tool for signal processing and finds numerous applications in various fields such as audio compression, pattern recognition, texture discrimination, computer graphics [12-14] etc. Specifically the 2-D DWT and its counterpart 2-D Inverse DWT (IDWT) play a significant role in many image/video coding applications.

III. DISCRETE WAVELET TRANSFORM

There are some differences in designing filters in filter banks compared with wavelet transforms. Wavelet filters are designed using associated continuous scaling functions and iterations. The filters in filter banks do not have to be associated with a single filter or basis function. They can be designed and optimized in many ways. However, the most commonly used image compression systems employ filters with Perfect Reconstruction (PR), Finite Impulse Response (FIR), and linear phase, and they are nonunitary (biorthogonal). The Pyramid Algorithm Analysis developed by Mallat is one of the most successful DWT algorithms. Mallat shows that the DWT can be viewed as a multi-stage signal decomposition process using the basic filter bank structure shown in Fig. 1.

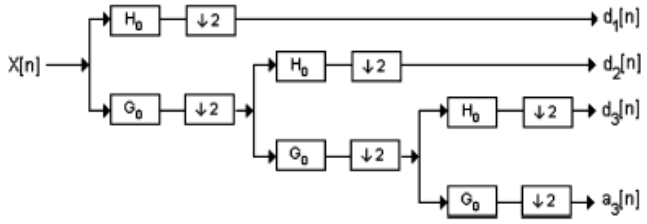

Fig.1 Three Level Wavelet Decomposition Structure

In this implementation the input signal is decomposed into its coarse approximation coefficients from the low-pass filter channel and its detail coefficients from the high-pass filter channel. Down sampling is applied after filtering the signal through the analysis filter bank to remove the redundancy introduced when a single length input is converted to a double length output. The filter bank operates recursively on the low-pass filtered data to generate coarser decompositions of the input signal and its corresponding details. Enhanced signal information and a better understanding of the signal behavior can be gained by observing the output of the signal at different levels of decomposition. Three stages of decomposition are usually considered sufficient for many applications.

IV. THE 1D DWT ARCHITECTURE

The 1D DWT levels 2 to 9 can, as already mentioned above, be used as components of a feature vector. This implies that the implementation of nine levels is necessary. In our experiment, only three levels of a 16- coefficients Daubechies orthogonal 1D DWT filter have been implemented. It should be noted that our implementation is scalable for different filter lengths and additional levels. For the polyphase structure, the filter coefficients are divided into even and odd parts. We represent the filter coefficients using the 2's complement, fixed point notation by incrementing the word length during the calculation to 18 bits so as to maintain a good SNR at the output.

A. FIR Filter Architecture

For image compression transformation is one of the important blocks. Next to this quantization and encoder are used for compressing the image. In the transformation part wavelet transform based FIR filter structure is used. The architecture of the FIR filter shown in Fig. 2 is based on the calculation unit structure and a Finite State Machine (FSM).The FSM controls the calculation unit and adapts to the actual filter length. This is important since it makes the architecture easily scalable. The fact that the choice of data source and operation mode of the FIR filter is completely controlled by the FSM makes it possible to use a single FIR filter sequentially instead of multiple filters in parallel.

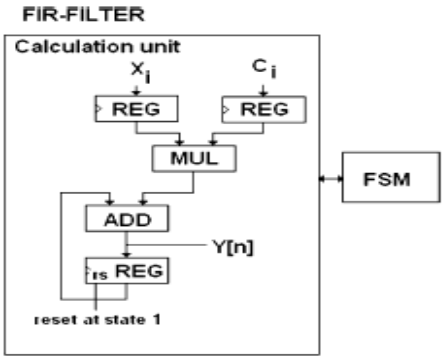

Fig.2 Proposed FIR Filter Architecture

This implies that only one FIR filter structure is required instead of all four filters. However, since this causes unnecessary delays together with the fact that the complete structure is quite small, two FIR filters are proposed in our approach—one acting on the high pass section and the other on the low pass section, as shown in Fig. 3

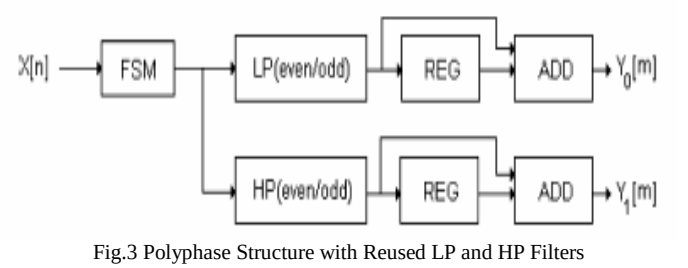

Fig.3 Polyphase Structure with Reused LP and HP Filters

B. The Proposed Architecture

The proposed architecture used for the three-level 1D DWT comprises two FIR-filter structures, three FSM controls, memory units, adders, registers and multiplexing switches.Fig.4 shows the block diagram of the system architecture. This architecture uses the polyphase structure along with the calculation unit structure. In this architecture, even samples are calculated on even clock cycles and the odd samples are calculated on the odd clock cycles. Usually, FIR filters have to maintain the previous (N-1) samples in memory for an N-length filter and they generally have separate register banks connected to them. In our design, a RAM based sample storage was constructed, which reserves an array of N memory cells for each instance ((level1), LP (level1), (level2), etc.) of the filter and then stores each incoming sample by replacing the oldest in the memory giving its address as the starting point to the filter. After the last sample in the linear array the first sample will be processed, creating a circular structure. Thus, the implementation uses a circular first in first out (FIFO) queue for data storage. The filter also requires a start address to the appropriate filter bank. The design contains two separate ROMs for the LP and HP filter coefficients and two separate registers for the addresses indicating the coefficients to be used. A three-level 1D DWT structure requires an FSM in order to control the two FIR filters.

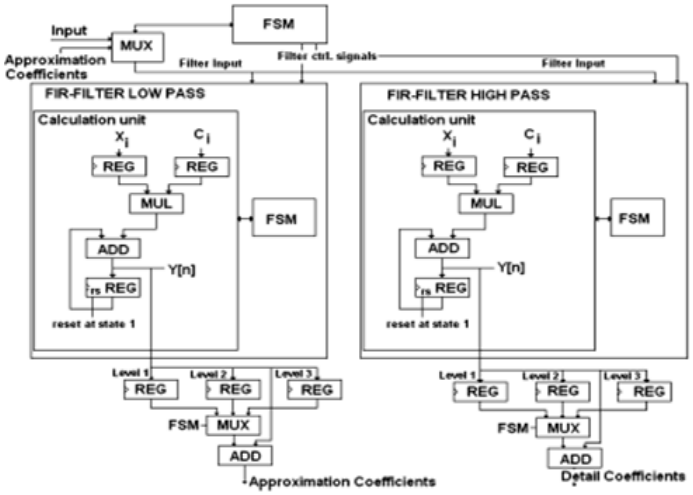

Fig. 4. Proposed System Architecture with Two FIR Filters,
One Acting on the High Pass Section and Another on the Low Pass Section

The FSM maintains control over the samples received and decides whether they are even or odd; it then signals the FIR filters indicating the memory address starting point that can be used. This is performed by counting the samples with a counter.

A three-level 1D DWT requires a type of control system that can indicate when to calculate on level one and when to calculate on the others. This is performed by looking at the numbers obtained from the counter. The counter only needs to calculate up to the filter length and then it can start over as the process repeats itself. Thus three levels are used for transformation of image signal using wavelet transform and next step is quantization and encoding. The amount of data after performing a3-scale wavelet decomposition is still the same as that contained in the original image. However we are now in a position to look at the quantization and coding of this output data (wavelet coefficients).

A wavelet transform using a desired number of scales is applied to the image pixels. The wavelet coefficients (transform output) are organized in a certain way, quantized and entropy encoded, resulting in a bit stream. For decoding, the reverse is done. The encoded bit skeam is entropy decoded and inverse quantization is carried nut to recover the wavelet coefficients, organized in the same way as for encoding. Then the coefficients are inverse-transformed to reconstruct the image pixels

V. SIMULATION RESULT

Filters are used as the basis for certain classes of wavelet decomposition methods used in modern image compression systems. In order to quantify the performance of the implemented architecture, we conducted several tests using different sets of input data.

1) Original Image

2) Approximated Image

3) Compressed Image

VI. CONCLUSION

This research article presents a design framework for the implementation of the One-Dimensional discrete wavelet transform on FPGA using a polyphase structure. The wavelet transform produces larger compression ratios with smaller Root-Mean-Square Error values than the Discrete Cosine Transform Discrete Cosine Transform or Fast Fourier Transform. Taking multiple levels and higher order transforms produces better results. Initiatively I have been implemented the three-level 1D DWT for this research. However, it should be highlighted that the proposed architecture is highly scalable to different filter lengths and additional levels.

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