INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) www.irjaet.com

ISSN (PRINT) : 2454-4744 | ISSN (ONLINE): 2454-4752

Vol. 1, Issue 4, pp.246 - 252, November, 2015

A RELIABLE LOW POWER MULTIPLIER DESIGN BY ADOPTING ANT ARCHITECTURE WITH FIXED WIDTH MULTIPLIER

A.Mani[1] | V.Sakthivel[2]

PG student, Paavai Engineering college, Namakkal

Asst professor, Paavai Engineering college, Namakkal

ARTICLE INFO

Article History:

Received 21st Nov, 2015

Received in revised form 23rd Nov,2015

Accepted 25th Nov, 2015

Published online 29th Nov, 2015

Keywords:

Algorithmic noise tolerant (ANT), fixed-width multiplier, reduced-precision replica (RPR), voltage overscaling (VOS)

ABSTRACT

In this paper, proposed An Area Efficient Multiplier De-sign Using Fixed-Width Replica Redundancy by adopting algorithmic noise tolerant (ANT) architecture with the fixed-width multiplier to build the reduced precision replica redundancy block (RPR). The proposed ANT architecture can meet the demand of high precision, low power consumption, and area efficiency. We design the fixed-width RPR with error compensation circuit via analysing of probability and statistics. Using the partial product terms of input correction vector and minor in-put correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified. In a 16 × 16 bit ANT multiplier, circuit area in our fixed-width RPR can be lower and power consumption in our ANT design can be saved as com-pared with the state-of-art ANT design.

1. INTRODUCTION

The raid growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. To lower the power dissipation, supply voltage scaling is widely used as an effective low-power technique since the power consumption in CMOS circuits is proportional to the square of supply voltage. However, in deep-sub micrometer process technologies, noise interference problems have raised difficulty to design the reliable and efficient microelectronics systems; hence, the design techniques to enhance noise tolerance have been widely developed.

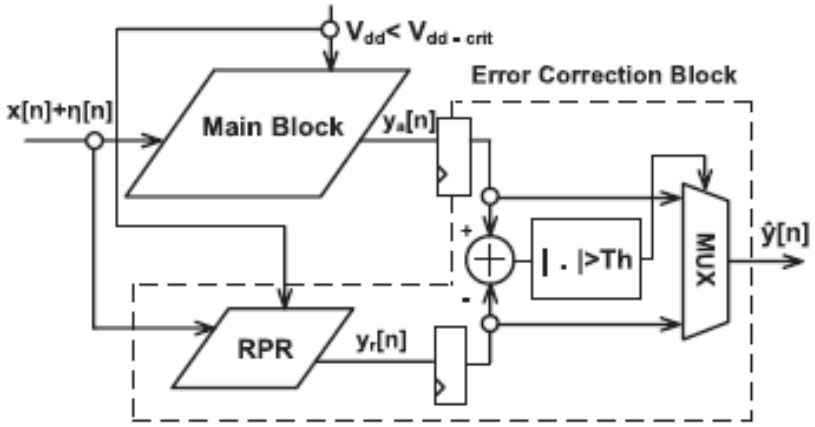

Fig.1. ANT Architecture

The RPR designs in the ANT designs can operate in a very fast manner, but their hardware complexity is too complex. As a result, the RPR design in the ANT design of [2] is still the most popular design because of its simplicity. However, adopting with RPR in [2] should still pay extra area overhead and power consumption. In this paper, we further proposed an easy way using the fixed-width RPR to replace the full-width RPR block in [2]. Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead. We take use of probability, statistics, and partial product weight analysis to find the approximate compensation vector for a more precise RPR design. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path. As a result, we can realize the ANT design with smaller circuit area, lower power consumption, and lower critical supply voltage.

2. ANT ARCHITECTURE DESIGINS

In this paper, we further proposed the fixed-width RPR tore place the full-width RPR block in the ANT design [2],as shown in Fig.2, which can not only provide higher computation precision, lower power consumption, and lower area overhead in RPR, but also perform with higher SNR, more area efficient, lower operating sup-ply voltage, and lower power consumption in realizing the ANT architecture. We demonstrate our fixed-width RPR-based ANT design in an ANT multiplier. The fixed-width designs are usually applied in DSP applications to avoid infinite growth of bit width. Cutting off n-bit least significant bit (LSB) output is a popular solution to construct a fixed-width DSP with n-bit input and n-bit output. The hardware complexity and power consumption of a fixed-width DSP is usually about half of the full-length one.

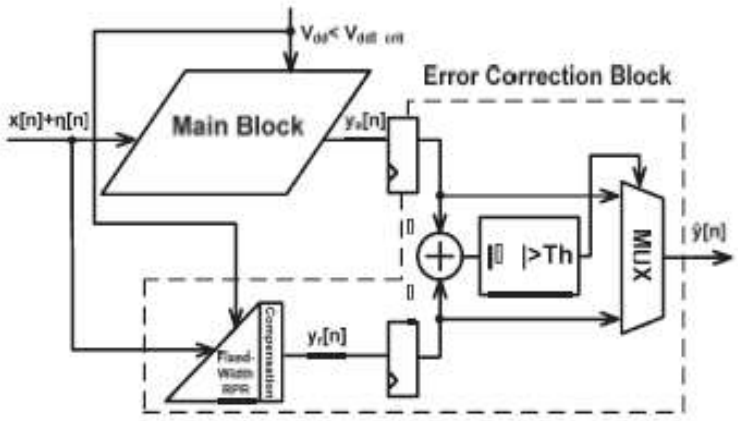

Fig.2. Proposed ANT architecture with fixed-width RPR

In nowadays, there are many fixed-width multiplier designs applied to the full-width multipliers. However, there is still no fixed-width RPR design applied to the ANT multiplier designs. To achieve more precise error compensation, we compensate the truncation error with variable correction value. We construct the error compensation circuit mainly using the partial product terms with the largest weight in the least significant segment. The error compensation algorithm makes use of probability, statistics, and linear regression analysis to find the approximate compensation value. To further lower the compensation error, we also consider the impact of truncated products with the second most significant bits on the error compensation. We propose an error compensation circuit using a simple minor input correction vector to compensation the error remained. In order not to increase the critical path delay, we locate the compensation circuit in the non-critical path of the fixed-width RPR. As compared with the full-width RPR design in , the proposed fixed-width RPR multiplier not only performs with higher SNR but also with lower circuitry area and lower power consumption. Therefore, they can be applied to construct the truncation error compensation algorithm.

3. PROPOSED ANT MULTIPLIER DESIGN USING FIXED-WIDTH RPR

In the ANT design, the function of RPR is to correct the errors occurring in the output of MDSP and maintain the SNR of whole system while lowering supply voltage. In the case of using fixed-width RPR to realize ANT architecture, we not only lower circuit area and power consumption, but also accelerate the computation speed as compared with the conventional full-length RPR. However, we need to compensate huge truncation error due to cutting off many hardware elements in the LSB part of MDSP

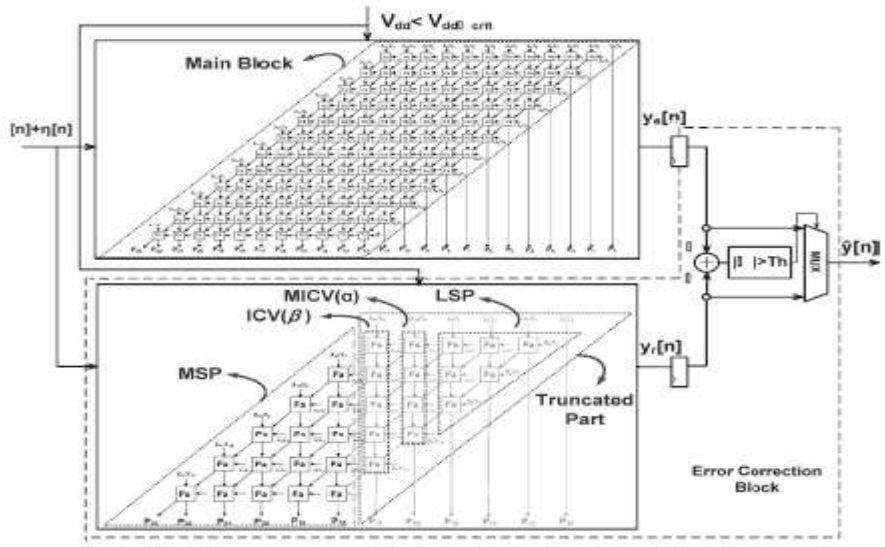

Fig. 3. 12 × 12 bit ANT multiplier is implemented with the six-bit fixed width replica redundancy block

In the MDSP of n-bit ANT Baugh–Wooley array multiplier, its two unsigned n-bit inputs of X and Y can be expressed as

$$X = \sum_{i=0}^{n-1} x_i \cdot 2^i, \qquad Y = \sum_{j=0}^{n-1} y_j \cdot 2^j.$$

The multiplication result P is the summation of partial products of xi y j , which is expressed as

$$P = \sum_{k=0}^{2n-1} p_k \cdot 2^k = \sum_{j=0}^{n-1} \sum_{i=0}^{n-1} x_i y_j \cdot 2^{i+j}.$$

The (n/2)-bit unsigned full-width Baugh–Wooley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(β)], minor ICV [MICV(α)], and LSP, as shown in Fig. 3. In the fixedwidth RPR, only MSP part is kept and the other parts are removed. Therefore, the other three parts of ICV(β), MICV(α), and LSP are called as truncated part. The truncated ICV(β) and MICV(α) are the most important parts because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm. The source of errors generated in the fixed-width RPR is dominated by the bit products of ICV since they have the largest weight. it is reported that a low-cost EC circuit can be designed easily if a simple relationship between f (EC) and β is found. It is noted that β is the summation of all partial products of ICV.

4. OUTPUT RESULT ANALYSIS

To evaluate and compare the performance of the proposed fixed-width RPR based ANT design and the previous full width RPR-based ANT design, we implemented these two ANT designs in a 12-bit by 12-bit multiplier. The main performance indexes are the precision of RPR blocks, the silicon area of RPR blocks, the critical computation delay of RPR blocks, the error probability of RPR blocks under VOS, and the lowest reliable operating supply voltage under VOS. Through quantitative analysis of experimental data, we can demonstrate that our proposed design can more effectively restrain the soft noise interference resulting from postponed computation delay under VOS when the circuit operates with a very low-voltage supply.

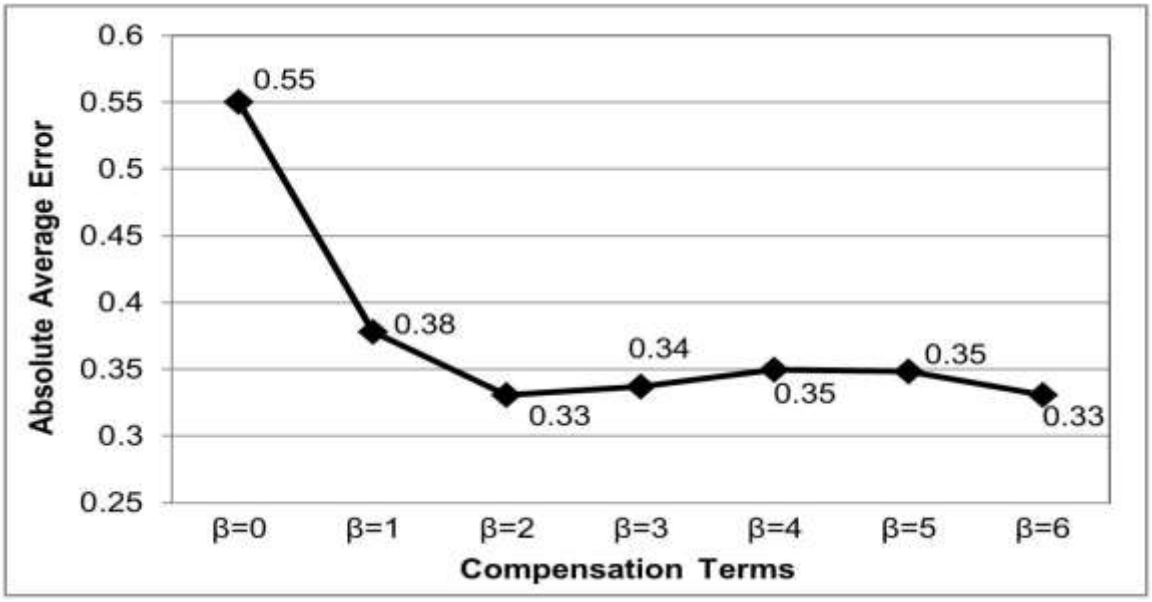

Fig.4. Analysis of absolute average compensation error under various β values in the 12-bit fixed-width RPR-based ANT multiplier

To evaluate the signal quality performance of various designs under VOS, we compare the error probability of various RPR blocks under VOS by injecting 10 000 input random patterns as test bench. Here, we follow the definition of the VOS factor, Kvos, defined in to identify the level of the supply voltage can be reliably lowered. The Kvos is ranged from one to zero. To further identify the lowest achievable reliable Kvos, we compare the output SNR of various RPR designs under different Kvos. To lowering supply voltage beyond critical supply voltage without sacrificing the throughput and without leading to severe SNR degradation, the critical computation delay in the RPR block must be as fast as possible. The shorter computation delay in RPR can bring the benefits of lower overscaling supply voltage adopted. To determine the optimized bit-length of fixed-RPR, comparisons of the Kvos and RPR area with different bit length of RPR block. Our goal is to select the bit length of fixed-RPR, which can achieve the lowest Kvos. The smaller RPR can perform with higher speed, lower power consumption,

and lower area. However, RPR with lower bit length would also lead to SNR degradation. Therefore, a tradeoff between hardware area and RPR bit length is needed. In this paper, the optimized bit length of fixed-RPR is selected as six based on the lowest Kvos analysis results.

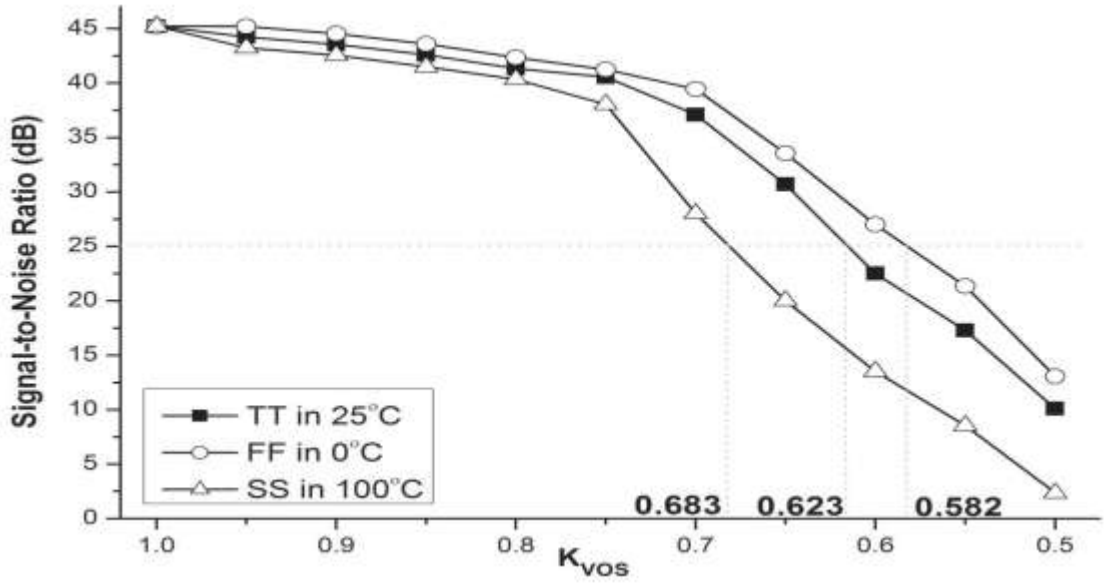

Fig.5. Comparisons of the output SNR of various process corners under different Kvos

Therefore, the lowest power saving in the proposed design can achieve 68%, while the full-width RPR-based ANT design can achieve 62%. The desirable SNR here is expected to be 25 dB. For the case the system requirement in signal quality is higher than 25 dB, the merits in these designs can still be maintained.

CONCLUSION

In this paper, a low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. The proposed 12-bit ANT multiplier circuit is implemented in TSMC 90-nm process and its silicon area is 4616.5 ìm2. Under 0.6 V supply voltage and 200-MHz operating frequency, the power consumption is 0.393 mW. In the presented 12-bit by 12-bit ANT multiplier, the circuitry area in our fixed-width RPR can be saved by 45%, the lowest reliable operating supply voltage in our ANT design can be lowered to 0.623 VDD, and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

REFERENCES

[1] (2009). The International Technology Roadmap for Semiconductors [Online]. Available: http://public.itrs.net/

[2] B. Shim, S. Sridhara, and N. R. Shanbhag, “Reliable low-power digital signal processing via reduced precision redundancy,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 497–510, May 2004.

[3] B. Shim and N. R. Shanbhag, "Energy-efficient soft-error tolerant digital signal processing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 4, pp. 336–348, Apr. 2006.
[4] R. Hedge and N. R. Shanbhag, "Energy-efficient signal processing via algorithmic noise-tolerance," in Proc. IEEE Int. Symp. Low Power Electron. Des., Aug. 1999, pp. 30–35.
[5] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," IEEE Trans. Comput. Added Des. Integr. Circuits Syst., vol. 32, no. 1, pp. 124–137, Jan. 2013.
[6] Y. Liu, T. Zhang, and K. K. Parhi, "Computation error analysis in digital signal processing systems with overscaled supply voltage," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 18, no. 4, pp. 517–526, Apr. 2010.
[7] J. N. Chen, J. H. Hu, and S. Y. Li, "Low power digital signal processing scheme via stochastic logic protection," in Proc. IEEE Int. Symp. Circuits Syst., May 2012, pp. 3077–3080.
[8] J. N. Chen and J. H. Hu, "Energy-efficient digital signal processing via voltage-overscaling-based residue number system," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 1322–1332, Jul. 2013.
[9] P. N. Whatmough, S. Das, D. M. Bull, and I. Darwazeh, "Circuit-level timing error tolerance for low-power DSP filters and transforms," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 21, no. 6, pp. 12–18, Feb. 2012.
[10] G. Karakonstantis, D. Mohapatra, and K. Roy, "Logic and memory design based on unequal error protection for voltage-scalable, robust and adaptive DSP systems," J. Signal Process. Syst., vol. 68, no. 3, pp. 415–431, 2012.