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ANALYZE THE ENERGY EFFICIENT AND POWER DISSIPATION USING DIGITAL FIR FILTERS

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Abstract – The Non-recursive filters are widely used in communications and Digital signal processing applications. Along with the recent trends in VLSI technology as the signal processing has become increasingly popular in the high speed realization of FIR filters with low power consumption. This paper mainly focused on the complexity of implementation grows with the filter orders, precision of computation and real-time realization of these filters with desired level of accuracy is a challenging task. To guarantee that no dynamic power is dissipated in the active sub-Luck up tables, the corresponding sub-LUT addresses are latched and remain constant throughout a particular operation. In addition to this, MAC units are added to increase the speed of architecture. The results are demonstrated by evaluating the area and performance, power dissipation of FIR filter configurations comprising one and two MAC units.

Keywords - *FIR digital filters, DSP, LUT , MAC unit*

I. INTRODUCTION

Most portable electronic devices such as cellular phones, personal digital assistants, and hearing aids require digital signal processing (DSP) for high performance. Due to the increased demand of the implementation of sophisticated DSP algorithms, low-cost designs, low area and power cost, are needed to make these handheld devices.

Finite Impulse Response (FIR) digital filters can be realized in parallel using as many multipliers as the number of coefficients in the filter. But multiplier consumes more power. The alternate approach for multiplication is done by performing addition operation. New algorithms based on LNS which aims specifically at addition and subtraction functions are introduced which can significantly improve the overall performance of an arithmetic system.

II. LOGARITHMIC NUMBER SYSTEM

The dominant component of power dissipation for well-designed CMOS circuits of dynamic power dissipation is given by,

$$P = aC_L V_{dd}^2 f \qquad (1)$$

where a is activity factor, C_L is the switching capacitance, f is the clock frequency and Vdd is the supply voltage. A variety of design techniques are commonly employed to reduce the factors of product without degrading the system. Higher design abstraction levels aim to reduce the computational load and the number of memory accesses required to perform a certain task and to introduce parallelism and pipelining in the system. At circuit and process levels, minimal feature size circuits are preferred capable of operating at minimal supply voltages while leakage currents and device threshold voltages are minimized.

The application of computer arithmetic techniques namely the LNS and RNS can reduce power dissipation by minimizing particular factors. where LNS and RNS are the two classes of transformation namely the Logarithmic Number System and Residue Number System.

III. PROPOSED METHOD

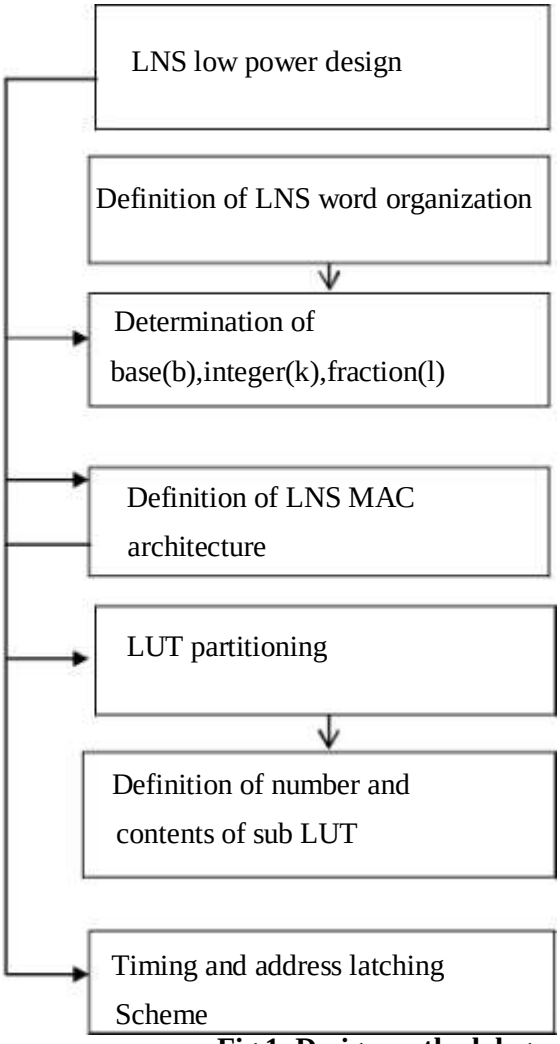

Fig.1. Design methodology

A low-power design framework for LNS systems is proposed. The quantification of power dissipation reduction and performance improvement made possible by using a LNS, compared to equivalent binary implementations in a contemporary 90-nm technology.Subsequently, in the second stage of the proposed framework the design techniques and the derived architectures are presented, targeting LNS MAC units in 90-nm technology. To illustrate the use of the proposed framework, the area-time-power design space of a low-pass finite impulse response (FIR) filter is explored for configurations of MAC units.

IV.DESIGN OF LNS CIRCUITS

There are two main approaches to implement the evaluation of functions, namely the hardware implementation of an approximation algorithm or the offline precomputation and storage of all required values in an LUT. The former approach is generally adopted for high-precision applications, while the latter approach is generally preferable for smaller word lengths, i.e., in relatively low-precision applications where the size of the required LUTs is moderate. The organization of an LNS adder/subtractor investigated, distinguished by two choices, i.e., first, the choice of using either latches or D flip-flops (DFFs) and second, the choice to select the active sub-LUT either based on MSB or LSB.Further power dissipation reduction is sought at the implementation of MAC units, by using retiming techniques, as well as at the algorithmic optimization level .Assume that b denotes the logarithmic base and l is the number of the fractional bits employed in the representation of the logarithms. The values required to be stored in the memory subsystem,

$$W(b,1)=[X_{eff}/2^{-1}] \qquad (2)$$

Fewer bits per entry are required to be stored in LUT2 than in LUT1. Sub-LUTs that correspond to the upper parts of the interval, need to store data words of reduced length, since stored values share a common most significant part.The above analysis reveals that the partitioning of the storage into sub-LUTs with latched inputs, introduces an area cost for latching the sub-LUT addresses and multiplexing the sub-LUT outputs. The particular complexity increases linearly with the number N of sub-LUTs.

Direct Lookup Table

Partitioning is often combined with an interpolation scheme. Instead of using a single uniform partition (direct lookup table approach), the technique can be realised by segregating the ROM into various sizes of interval mapping with the domain function of addition and subtraction algorithms.

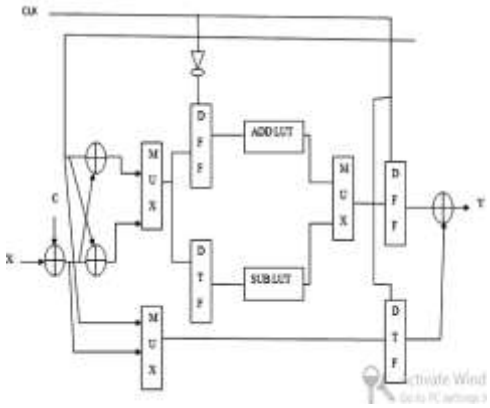

Fig.2. Retimed LNS MAC unit

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These intervals are distributed in smaller regions with similar widths of partition endpoints, hence providing substantial savings in ROM area.

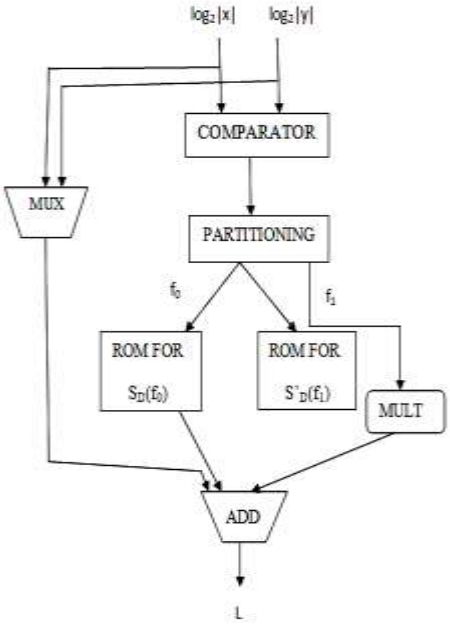

Fig.3. LNS adder implemented using linear interpolation

LNS system that uses bipartite tables will require significantly less memory than one thatuses conventional lookup tables. Moreover, apart from only involving an additionoperation at the final stage, the technique often has shorter overall delays since thesmaller tables have shorter access times too.

Word Length Determination

By optimizing LNS representation parameters with the objective to achieve a particular SNR, low-power operation can be achieved. It is noted that does not take into account coefficient quantization and overflow/underflow errors. The latter implies no limit on the number of integral bits. The organization of the LNS word, i.e., the total word length and the partitioning of the LNS word into k integer and l fractional bits, is determined using the experimental methodology.

V.LNS MAC AND FIR IMPLEMENTATION ISSUES

The basic structure of the single-MAC unit. An FIR filter is described by ,

$$Y(n)=\sum_{i=0}^{N-1} C \qquad (3)$$

where C_i is the filter coefficients, X(n-i) is the input sequence and Y(n) is the output sequence.i

Y

Multiplier Adder

Fig.4.Organization of single MAC architecture

Retimed MAC Unit

A solution of switching activity problem is solved by retime the circuit so that the register located at the feedback path is replaced by registers placed at the inputs of the final adder. The amount of the switching activity depends on the logic depth of the LUT implementation. The Power dissipation in retimed circuit is more efficient.

Hence, the retimed circuit is adopted for the LNS MAC implementations. The LUTs have been implemented as combinational logic, synthesized in a UMC 90-nm 1.0V CMOS standard cell library, by using the Synopsys Design Compiler. It is noted that alatch-based gated clock is used for the DFFs, since additional signals are used to enable the corresponding flip-flops.

Since the utilization of the MSB for LUT selection is not efficient for a latch-based design due to additional hardware used to introduce the required delay to fast paths of the circuit, a solution based on DFFs is preferable. Moreover, the flip-flop-based selection is better supported by commercial EDA design flows. The advantage is that it is easier to resolve time violations.

VI.RESULTS AND DISCUSSION

The Block diagram of the LNS architecture is coded in VHDL is mainly discussed about the whole Architecture is split into several sub modules, each sub modules are then coded separately and are instantiated in the main module.

Then the code is compiled and synthesized using Xilinx ISE 13.4 Design Suite and is simulated using the Isim 13.4 software. Then the power, Area and throughput is compiled in design compiler using Synopsys tool.In addition, the design flows of the simulation and synthesis are also processed.

Timing Evaluation

The main purpose of performing timing analysis is to investigate the delaycharacteristics, in terms of maximum or minimum delays, that occur in a design. Conversely, the shortest signalpropagation delay path in a combinational circuit represents the minimum delay inthe system.

The simulation of MAC unit, multiplexer unit, LNS adder/subtractor units are described in verilog language and the simulation is done in Isim13.4 and the code is functionally verified to be correct.

Area Estimation

One of the design criteria currently receiving increased attention is the size of acircuit. A smaller total area can lead to the best implementation due to incurring lower costs. An exact estimation of the area is normally calculated after a circuit has been placed and routed.

VI.SIMULATION AND SYNTHESIS RESULT

Fig.5.Simulation of DFF

The above fig.shows the simulation result of delay flip flop which enabled while clock cycle is positive and reset is zero.The output of this flipflop is same as input but it takes some delay.

Fig .6.Simulation of MAC

The above figure shows a simulation result of multiply and accumulate unit which is used to increase the speed of the architecture.The multiplied value is added to the accumulator value and the result is stored in accumulator.

Fig.7. shows simulation result of FIR filter which produces output only when reset is zero and positive cycle of clock pulse

Fig.8.Simulation of 2-sub LUT

Fig.8..shows the simulation result of 2sub LUT which is enabled only when clock cycle goes high.The values are stored in two lookup table for reducing a power and it is accessed using the address value.

Fig.9.Power report of 2-sub LUT

Fig.10.shows the xilinx power report of four sub LUT which consumes less power than the Fig.9.

Fig.10.Power report of 4-sub LUT

Table.2. Area of 1-MAC Vs 2-MAC

SUB LUT	1-MAC(nm)	2-MAC(nm)
2	55510.589542	71628.546941
4	57923.796558	89789.811000

Table.2. shows the comparison between area of single MAC architecture and 2-MAC architecture. The above table shows area has been increased while increasing the partition of lookup table.

Table.3.Power of 1-MAC Vs 2-MAC

SUB LUT	1-MAC(mW)	2-MAC(mW)
2	3.8160	0.4230
4	1.0868	0.3610

Table.3. shows the comparison between power of single MAC architecture and 2-MAC architecture. Hence proved the power dissipation is reduced while increasing the partition of lookup table.

VII.CONCLUSION

The adoption of LNS can lead to very efficient circuits for digital filter pplications when properly selecting the logarithmic base and the word length in a contemporary 90nm technology. Partitioning of the LUTs are employed to create parts in the circuit that can be independently activated, which, reduces power dissipation. Power has been reduced by latching the inputs to the LUTs. Also, the gated clock technique has been used to further reduce power consumption performed to the latched inputs due to the clock signal. The choice of number of sub-LUTs is an important design parameter that can be employed for exploration of the power design space, area and time. Furthermore, the application of retiming is particularly useful in avoiding unnecessary switching activity, due to unbalanced delay/latency paths in LNS arithmetic circuits. Finally, the high speed realization of FIR filter with low power consumption is obtained by while increasing the area of proposed LNS MAC architecture

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