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SIMULATION AND SHORT CHANNEL EFFECT ANALYSIS OF InAlN/GaN MOSHEMT WITH lnGaN BACK BARRIER

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Abstract:

In this present work of InAlN/GaN high-electron mobility transistor (HEMT) with a three-terminal OFF-state breakdown voltage (BV) and a low specific on-resistance. To suppress the short-channel effects (SCEs), an InGaN back barrier is applied in an InAlN/GaN hetero structure. To reduce the drain-to-source leakage current in this device, an InGaN back barrier has been used. The gate leakage current in these devices is owing to use of a SiO_2 layer . This current level is more than six orders of magnitude lower than in Schottky-barrier HEMT. The combination of InGaN back barrier, the high charge sheet density of InAlN/GaN HEMTs, and the low leakage because of the gate-dielectric layer allows for a figure-of-merit BV/*R*ON,SP. In a gate-length device with on-resistance and an extrinsic transconductance , a peak f_T is achieved. An electron velocity was extracted by two different delay analysis methods.

Keywords- Back barrier, current gain cutoff frequency(f_T), GaN, metal oxide semiconductor high-electron-mobility transistor (HEMT), InAlN,InGaN, short-channel effect (SCE),Break down voltage.

1. INTRODUCTION

The combination of high electron mobility and large breakdown voltage make GaN an ideal candidate to high-speed and high-power application. AlGaN/GaN high electron-mobility transistor (HEMT) with sio_2 gate oxide layer have traditionally led this field, and they have demonstrated an outstanding radiofrequency($R_{F)}$ performance with 225 GHz current gain cutoff frequency and 300 GHz power gain cutoff frequency(f_{max}) . However, device scaling below 50-nm gate length (L_g) is very challenging in AlGaN/GaN heterostructures because of difficulty in maintaining a sufficiently high aspect ratio (*Lg/d*, where *d* is the barrier thickness) to suppress short-channel effects (SCEs). Gate recess etching is used to improve aspect ratio; however, the dry etching process required the gate recess can induce damage in the channel as well as non uniformities across the wafer. In general, the breakdown voltage (BV) in HEMT devices scales with gate-to-drain distance (L_{gd}). However, increasing L_{gd} also increases the drain series resistance, which degrades the output power efficiency. To minimize the on-resistance, it is therefore desirable to select heterostructures with a high sheet charge density, although this can reduce the BV of the device.The InAlN/GaN HEMT is a promising high-power switching device with a potential for very low specific on-resistance carrier. In this letter, a 3.3-nm $In_{0.15}Ga_{0.85}N$ back barrier is used, instead of an AlGaN buffer, to increase the carrier confinement in InAlN/GaN HEMTs on SiC. The dc and RF performances of devices with gate length varying from 30 to 230 nm are investigated. In the 30-nm-gate-length device with an on resistance of 1.2 Ω ・ mm and an extrinsic transconductance of 530 mS/mm, an f_T of 300 GHz was achieved. This is the highest f_T reported so far in GaN-based transistors. An electron velocity in the 1.37–1.45 × 10^7 cm/s range was extracted in this device by two different methods.

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2. DEVICE FABRICATION

A simplified cross-sectional view of the fabricated InAlN/GaN MOSHEMTs with an InGaN back barrier is shown in Fig. 1. The lattice matched $In_{0.17}Al_{0.83}N$/GaN 3000-V 4.3-m$\Omega \cdot cm^2$ InAlN/GaN MOSHEMT with InGaN back barrier heterostructure is grown by metal–organic chemical vapor deposition on a semi-insulating SiC substrate[6]. After an AlN nucleation layer, a 0.85-μm 4% InGaN back barrier is deposited, followed by a 26-nm-thick GaN channel.. Then, ohmic contacts are formed with a metal stack deposition and subsequent annealing at 820 ◦C for 60 s. A contact resistance of 0.3–0.4 $\Omega \cdot$ mm is obtained. The source-to-drain distance is 1 μm. After the ohmic contact fabrication, an oxygen plasma is applied everywhere on the wafer for reduce the gate leakage current and to improve RF performance. This sio_2 forms a 1–2-nm oxide layer on top of the InAlN layer. Sub micrometer gates with lengths from 30 to 230 nm were defined in the middle of the source–drain region by electron-beam lithography. To study the impact of the InGaN back barrier, samples with a GaN buffer and no back barrier were also grown as control and the AlN

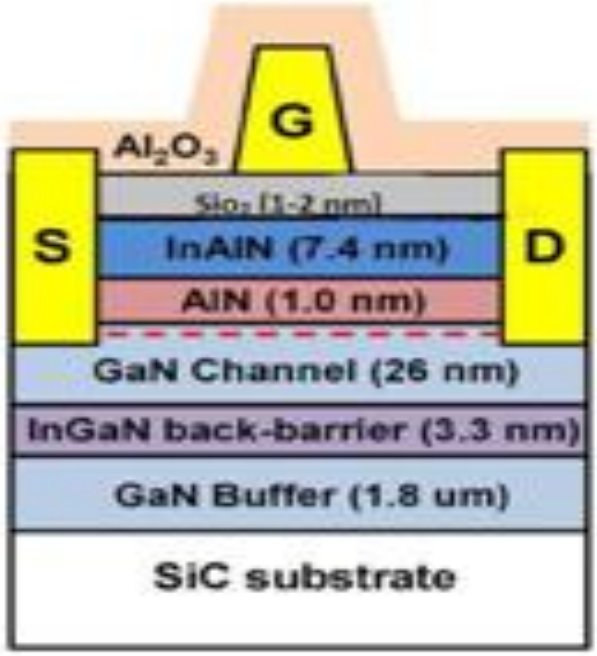

Fig.2.Device Fabrication

The thin AlN interlayer between the $In_{0.17}Al_{0.83}N$ layer and the GaN channel help to reduce interface roughness and improve two dimensional electron gas electron gas(2DEG) mobility . A total of 1.5 × 1013 cm^{-2} 2DEG charge density cm^{-2}, an electron mobility of 1389 $cm^2/V \cdot s$, and a sheet resistance of 290 Ω/_ are measured by the Hall technique at room temperature[2]. The device fabrication is started with mesa isolation, performed by electron-cyclotron-resonance etching with a plasma gas mixture. A 5 metal stack was evaporated on both source and drain regions after surface cleaning. The sample is then annealed in 850 ◦C for 30 s to form ohmic contacts.

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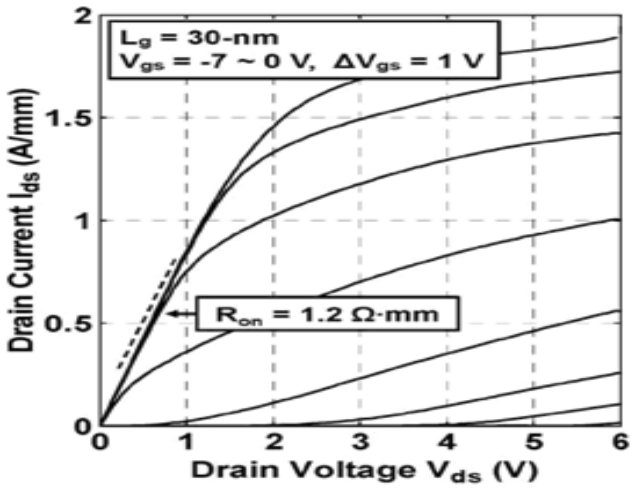

Fig.2. I_{ds} versus V_{ds} characteristics of the device with L_g = 30 nm

A contact resistance of 0.7 Ω · mm is measured by a transmission-line-method structure. After the cleaning and UV ozone treatment, a 13.5-nm thick sio$_2$was deposited by atomic layer deposition at 250 ◦C gate dielectric. Finally, a gate electrode was deposited in a high vacuum electron-beam evaporator. A reference Schottky barrier HEMT sample was prepared without a SiO_2 gate-dielectric layer to compare with the MOSHEMT devices. Finally, a gate electrode was deposited in a high vacuum electron-beam evaporator. A reference Schottky barrier HEMT sample was prepared without a SiO_2 gate-dielectric layer to compare with the MOSHEMT devices. The devices have a gate length L_g = 2 μm, gate width W_g = 100 μm, gate-to-source distance L_{gs} = 1.5 μm, and a gate-to-drain distance L_{gd} varied from 2 to 30 µm.

3. RESULTS AND DSCUSSION

The dc performance of the fabricated devices is characterized with a agilent 4155 parameter analyzer. In spite of the thick top barrier (9.4–10.4 nm), the combination of the back barrier and the thin GaN channel allow an effective suppression of the SCE down to 70-nm gate lengths; a small threshold of about 0.3 V was observed when the gate length was reduced from 250 down to 70 nm. However, as the gate length is scaled below 50 nm, the SCEs become evident, and the V_T decreases rapidly ($\Delta VT \approx 0.7$ V).

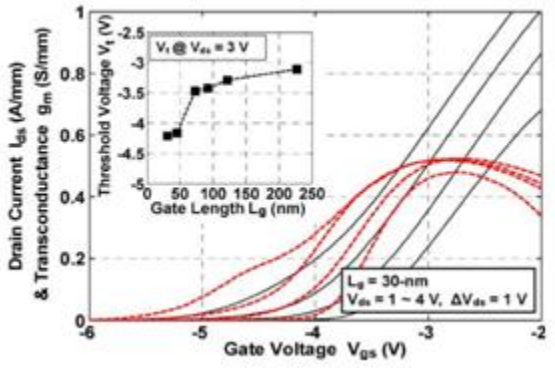

Fig.3. corresponding transfer curve at V_{ds} = 1−4

Fig. 3 shows the dc output and transfer characteristics of the InAlN/GaN MOSHEMTs with 30-nm gate length .At V_{gs} = 0 V, the device show a drain current over 1.8 A/mm with an on-resistance of 1.2 Ω ・ mm.

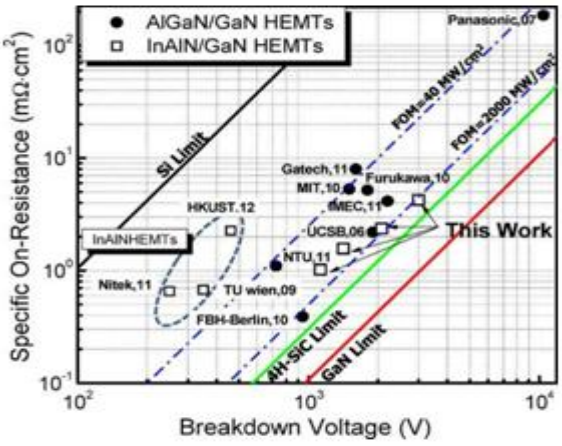

Fig.4. Specific on-resistance and BV of AlGaN/GaN and InAlN/GaN HEMTs

The peak extrinsic trans conductance of 520–530 mS/mm was obtained at V_{ds} = 2−4 V, and a threshold voltage (V_T) of −4.2 V is extracted at V_{ds} = 3 V. The f_T /f_{max} value before de-embedding are 200/34 GHz, respectively. As shown in the inset in Fig. 4, the $f_T \times Lg$ product decrease as the gate length scale down (17.3 GHz ・ μm for Lg = 230 nm and9.0 GHz μm for Lg = 30 nm). This decreases is mainly due to the total delay dominated by extrinsic and parasitic components. To extract the electron velocity to the device accurately, two different method are used. First, based on the delay analysis by Moll *et al*. [15], the parasitic charging delay was extracted at the effective bias condition [= *V*ds − *I*ds ・ (R_s + R_d)]. An electron velocity 1.37 × 107 cm/s is obtained from the slope of the plot of "total delay–parasitic charging delay" versus "gate length (L_g)," as shown in Fig. 6. As a second approach, the intrinsic gate capacitance (*C*gs.int and *C*gd.int) and *g*m.int were extracted from the small-signal S-parameter at the same bias condition used in the first method, and an electron velocity of1.45 × 107 cm/s was calculated from the slope of the intrinsic delay.

CONCLUSION

We have studied by the simulation of InAlN/GaN with InGaN back barrier (for mole concentration **x=0.17**) using MOSHEMT, where the effect of - InGaN back barrier layer on the device performance of the proposed structure of InAln/GaN Gate-Recessed Enhancement-Mode MOSHEMT. These results obtained from the simulations are compared with the previously reported results by other group of the device without back barrier layer. These device with **I**nGaN back barrier shows the excellent electrostatic control leading to obtain a very low gate leakage value. These device also shows a very high electron velocity of 1.37–1.45 × 10^7 cm/s.

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