INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

PERFORMANCE ANALYSIS OF PV BASED BOOST - SEPIC CASCADED INVERTER FED INDUCTION MOTOR SYSTEM USING PI & FLC

[1]Jasmine David, [2]Gopinath Mani,
[1]Research Scholar,Dept. Of Electrical and Electronics Engineering,St.Peter's University,Chennai,India
jas.malli@gmail.com,
[2]Professor,Dept. Of Electrical and Electronics Engineering,Dr.N.G.P Institute of Technology,Coimbatore,India.
mgopinath_10@yahoo.co.in.

Abstract:

This research work deals with comparison of PI and fuzzy logic control for boost to boost converter with SEPIC converter for induction motor drives which can be used in paper mills and textile mills. The performances analysis of Boost-Boost inverter fed IM drive system with boost SEPIC inverter fed IM drive system is validated by MATLAB Simulink. The boost - SEPIC converter is proposed to reduce the ripple in the input current. The output power of PV is boosted using a boost converter and applied to a seven level inverter. The results validated with these two controllers (PI and FLC) for boost to boost and boost – SEPIC system which conclude the boost – SEPIC converter with FLC will be suitable for this proposed work.

Keywords : SEPIC, FLC, PI, MATLAB.

1. INTRODUCTION

The extensive use of fossil fuels has resulted in the global problem of greenhouse emissions. Moreover, as the supplies of fossil fuels are depleted in the future, they will become increasingly costly. Thus, solar energy is becoming more important since it produces less pollution and the cost of fossil fuel energy is rising, while the cost of solar arrays is decreasing. In particular, small-capacity distributed power generation systems using solar energy may be widely used in residential applications in the near future [1], [2]. The power conversion interface is important to grid- connected solar power generation systems because it converts the DC power generated by a solar cell array into ac power and feeds this ac power into the utility grid. An inverter is necessary in the power conversion interface to convert the DC power to AC power [2]–[4]. Since the output voltage of a solar cell array is low, a DC–DC power converter is used in a small-capacity solar power generation system to boost the output voltage, so it can match the DC bus voltage of the inverter. The power conversion efficiency of the power conversion interface is important to in- sure that there is no waste of the energy generated by the solar cell array. The active devices and passive devices in the inverter produce a power loss. The power losses due to active devices include both conduction losses and switching losses [5]. Conduction loss results from the use of active devices, while the switching loss is proportional to the voltage and the current changes for each switching and switching frequency. A filter inductor is used to process the switching harmonics of an inverter, so the power loss is proportional to the amount of switching harmonics. The voltage change in each switching operation for a multi- level inverter is reduced in order to improve its power conversion efficiency [6]–[15] and the switching stress of the active devices. The amount of switching harmonics is also attenuated, so the power loss caused by the filter inductor is also reduced. Therefore, multilevel inverter technology has been the subject of much research over the past few years. In theory, multilevel inverters should be

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

designed with higher voltage levels in order to improve the conversion efficiency and to reduce harmonic content and electromagnetic interference (EMI). Conventional multilevel inverter topologies include the diode- clamped [6]–[10], the flying-capacitor [11]–[13], and the cascade H-bridge [14]–[18] types. Diode-clamped and flying- capacitor multilevel inverters use capacitors to develop several voltage levels. But it is difficult to regulate the voltage of these capacitors. Since it is difficult to create an asymmetric voltage technology in both the diode-clamped and the flying- capacitor topologies, the power circuit is complicated by the increase in the voltage levels that is necessary for a multilevel inverter. For a single-phase seven-level inverter, 12 power electronic switches are required in both the diode-clamped and the flying-capacitor topologies. Asymmetric voltage technology is used in the cascade H-bridge multilevel inverter to allow more levels of output voltage [17], so the cascade H-bridge multilevel inverter is suitable for applications with increased voltage levels. Two H-bridge inverters with a DC bus voltage of multiple relationships can be connected in cascade to produce a single- phase seven-level inverter and eight power electronic switches are used. More recently, various novel topologies for seven- level inverters have been proposed. For example, a single-phase seven-level grid-connected inverter has been developed for a photovoltaic system [18]. This seven-level grid-connected inverter contains six power electronic switches. However, three DC capacitors are used to construct the three voltage levels, which results in that balancing the voltages of the capacitors is more complex. In [19], a seven-level inverter topology, configured by a level generation part and a polarity generation part, is proposed is shown in figure 1.

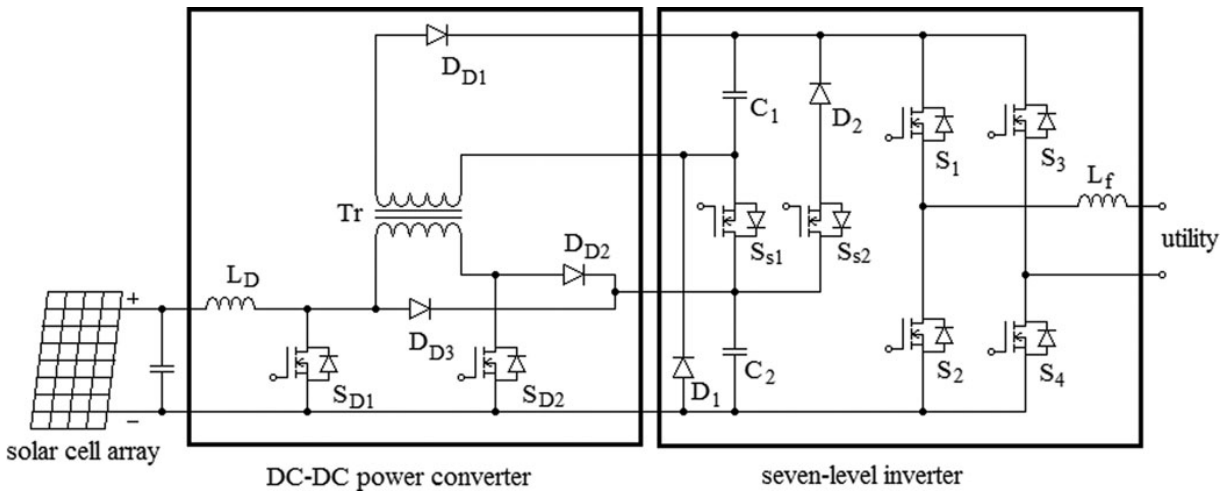

Figure: 1. Configuration of the solar power generation system.

There, only power electronic switches of the level generation part switch in high frequency, but ten power electronic switches and three DC capacitors are used. In [20], a modular multilevel inverter with a new modulation method is applied to the photovoltaic grid-connected generator. The modular multilevel inverter is similar to the cascade H-bridge type. For this, a new modulation method is proposed to achieve dynamic capacitor voltage balance. In [21], a multilevel DC-link inverter is presented to overcome the problem of partial shading of individual photovoltaic sources that are connected in series. The DC bus of a full-bridge inverter is configured by several individual DC blocks, where each DC block is composed of a solar cell, a power electronic switch, and a diode. Controlling the power electronics of the DC blocks will result in a multilevel DC-link voltage to supply a full-bridge inverter and to simultaneously overcome the problems of partial shading of individual

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

photovoltaic sources. According to the knowledge of authors, the boost to boost converter is not used between the PV system and multilevel inverter.

This paper compares the boost to boost converter and boost – SEPIC converter for PV system. The proposed solar power generation system is composed of a DC/DC power converter and a seven-level inverter. The seven- level inverter is configured using a capacitor selection circuit and a full-bridge power converter, connected in cascade. The seven-level inverter contains only eight power electronic switches, which simplifies the circuit configuration.

2. CIRCUIT CONFIGURATION

Figure.1 shows the configuration of the proposed solar power generation system. The proposed solar power generation system is composed of a solar cell array, a DC–DC power converter, and a new seven-level inverter. The solar cell array is connected to the DC–DC power converter, and the DC–DC power converter is a boost converter that incorporates a transformer. The DC–DC power converter converts the output power of the solar cell array into two independent voltage sources with multiple relationships, which are supplied to the seven level inverter. The seven –level inverter is composed of a capacitor selection circuit and a full bridge power converter, connected in a cascade. The power electronic switches of capacitor selection circuit determine the discharge of the two capacitors while the two capacitors are being discharged individually or in series. Because of the multiple relationships between the voltages of the DC capacitors, the capacitor selection circuit outputs a three-level DC voltage. The full-bridge power converter further converts this three-level DC voltage to a seven-level AC voltage that is synchronized with the utility voltage. In this way, the proposed solar power generation system generates a sinusoidal output current that is in phase with the utility voltage and is fed into the utility, which produces a unity power factor.

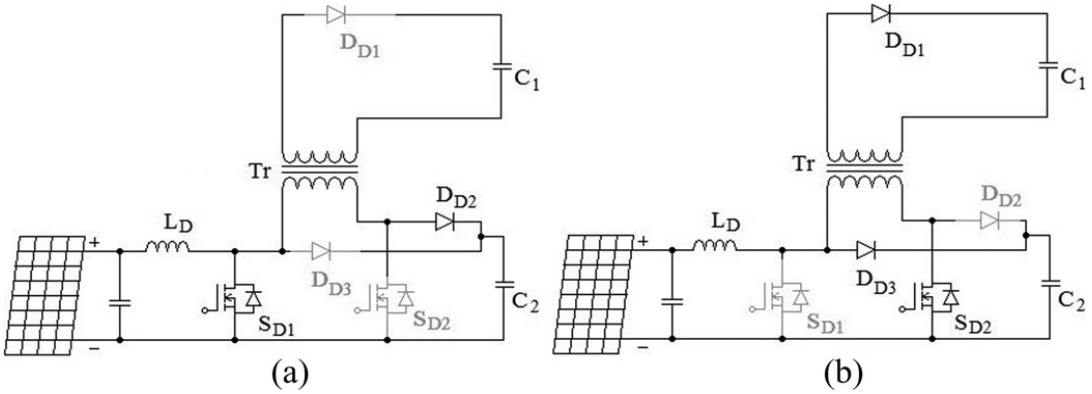

Figure: 2. Operation of DC–DC power converter: (a) $S_{D\ 1}$ is on and (b) $S_{D\ 1}$ is off.

3. DC-DC Power Converter

As seen in Figure 2. The DC-DC power converter incorporates a boost converter and a current fed forward converter. The boost converter is composed of an inductor L_D, a power electronic switch S_{D1}, and a diode, D_{D3}. The boost converter charges capacitor C_2 of the seven level inverter. The current fed forward converter is composed of an inductor LD, power electronic switches S_{D1} and S_{D2} ,a transformer and diode D_{D1} and D_{D2}. The current fed forward converter charges capacitor C1 of the seven level inverter. The inductor L_D and the power electronic switch SD1 of the current fed forward converter are also used in the boost converter.

Figure 2(a) shows the operating circuit of the DC-DC power converter when S_{D1} is turned on. The solar cell array supplies energy to the inductor L_D. When S_{D1} is turned off and S_{D2} is turned on, its operating circuit is shown in Figure 2(b). Accordingly, capacitor C_1 is connected to capacitor C_2 in

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

parallel through a transformer, so the energy of inductor L_D and the solar cell array charge capacitor C_2 through D_{D3} and charge capacitor C_1 through the transformer and D_{D1} during the off state of S_{D1}. Since capacitors C_1 and C_2 are charged in parallel by using transformer, the voltage ratio of capacitor C_1 and C_2 is the same as the turn ratio of the transformer. Therefore, the voltages of C_1 and C_2 have multiple relationships. The boost converter is operated in the Continuous Conduction Mode (CCM). The voltage of C_2 can be represented as

$$Vc2 = \frac{1}{1-D}.Vs \quad (1)$$

Where Vs is the output voltage of solar cell array and D is the duty ratio of S_{D1}. The voltage of capacitor C_1 can be represented as ,

$$Vc1 = \frac{1}{2(1-D)}.Vs \quad (2)$$

It should be noted that the current of the magnetizing inductance of the transformer increases when S_{D2} is in the on state. Conventionally, the forward converter needs a third demagnetizing winding in order to release the energy stored in the magnetizing inductance back to the power source. However in the proposed DC-DC power converter, the energy stored in the magnetizing inductance is delivered to capacitor C_2 through D_{D2} and S_{D1} when S_{D2} is turned off. Since the energy stored in magnetizing inductance is transferred forward to the output capacitor C_2 and not back to the DC source, the power efficiency is improved. In addition, the power circuit is simplified because the charging circuits for capacitors C_1 and C_2 are integrated. Capacitors C_1 and C_2 are charged in parallel by using the transformer, so their voltages automatically have multiple relationships. The control circuit is also simplified.

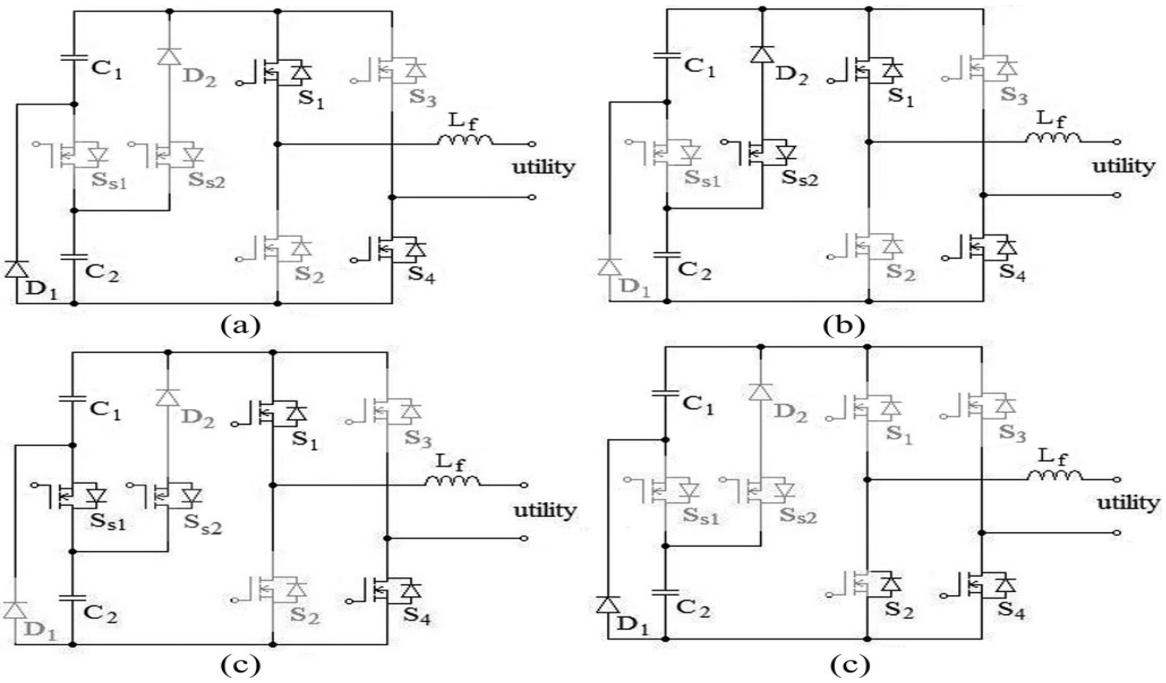

Figure: 3. Operation of the seven-level inverter in the positive half cycle, (a) mode 1, (b) mode 2, (c) mode 3, and (d) mode 4.

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

a) Proportional integral controller

The Proportional Integral controller is a basic solution for most industrial applications. It is popular because of its simple structure and can be easily implemented in practice in figure 4. The control action law of a PI controller is defined by the following equation:

$$u(t) = K_p e(t) + K_i \int_0^t e(t)dt \quad (3)$$

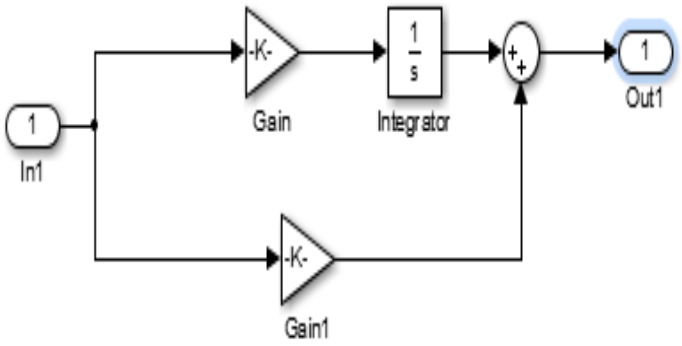

Figure: 4. Implementation of PI controller

b) Fuzzy logic controller

A Fuzzy Logic Controller (FLC) is basically designed by selecting its inputs and outputs, choosing the preprocessing needed for the inputs and de post – processing needed for the outputs, as well as designing each of its four basic components: Fuzzification, rule – base, inference mechanism and defuzzification (figure 10).

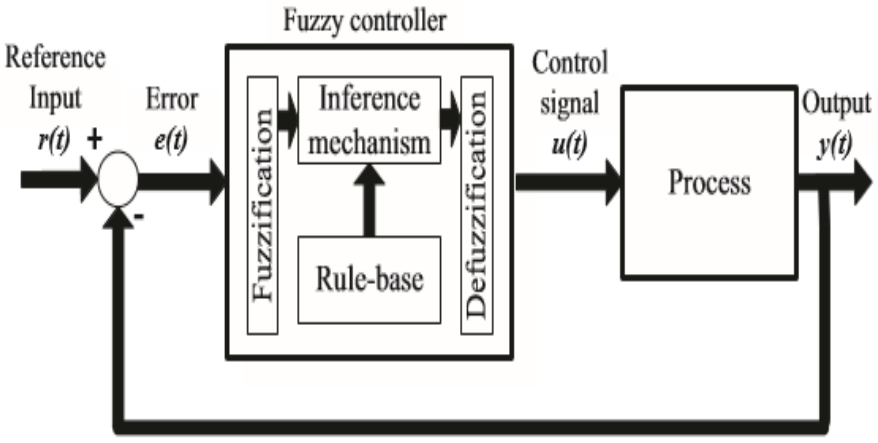

Figure: 5. An FLC is an artificial decision making system that operates in closed loop and real time as can be observed

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

e	Δe						
	nb	nm	ns	zr	ps	pm	pb
nb	nb	nb	nb	nm	nm	ns	zr
nm	nb	nb	nm	nm	ns	zr	ps
ns	nb	nm	nm	ns	zr	ps	pm
zr	nm	nm	ns	zr	ps	pm	pm
ps	nm	ns	zr	ps	pm	pm	pb
pm	ns	zr	ps	pm	pm	pb	pb
pb	zr	ps	pm	pm	pb	pb	pb

Table 1. Fuzzy Associate Memory for the Proposed System

4. PROPOSED BOOST – SEPIC CONVERTER

The single-ended primary-inductance converter (SEPIC) is a DC/DC-converter topology that provides a positive regulated output voltage from an input voltage that varies from above to below the output voltage. The coupled inductor not only provides a smaller footprint but also, to get the same inductor ripple current, requires only half the inductance required for a SEPIC with two separate inductors.

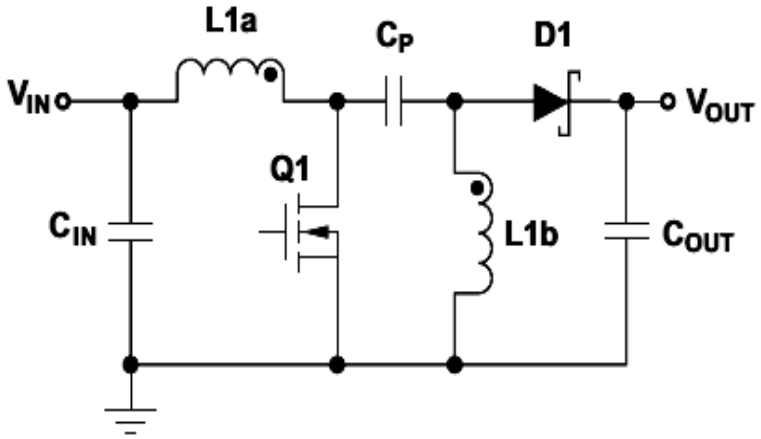

Figure 6: Proposed Boost - SEPIC Converter

Figure 1 shows a simple circuit diagram of a SEPIC converter, consisting of an input capacitor, C_{IN} an output capacitor, C_{OUT} coupled inductors L_1a and L_{1b} an AC coupling capacitor, C_P a power FET, Q_1 and a diode, D_1. it is important to analyze the circuit at DC when Q_1 is off and not switching. During steady-state CCM, pulse-width modulation (PWM) operation, and neglecting ripple voltage, capacitor CP is charged to the input voltage, VIN. When Q_1 is off, the voltage across L_{1b} must be V_{OUT}. Since C_{IN} is charged to V_{IN}, the voltage across Q_1 when Q_1 is off is V_{IN} + VOUT, so the voltage across L_{1a} is V_{OUT}. When Q_1 is on, capacitor C_P, charged to V_{IN}, is connected in parallel with L1b, so the voltage across L_{1b} is $–V_{IN}$. The currents flowing through various circuit components are shown in Figure 4. When Q1 is on, energy is being stored in L_1a from the input and in L1b from C_P. When Q_1 turns off, L1a's current continues to flow through C_P and D_1, and into C_{OUT} and the load. Both C_{OUT} and C_P get recharged so that they can provide the load current and charge L_{1b}, respectively, when Q_1 turns back on.

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

Duty cycle of boost -SEPIC converter can be determined by

$$D = \frac{V_{OUT} + V_{FWD}}{V_{IN+} V_{OUT} + V_{FWD}} \quad (4)$$

Where V_{FWD} is the forward voltage drop

5. SIMULATION RESULTS OF BOOST TO BOOST AND BOOST – SEPIC CONVERTER

The Seven level inverter based PV-Inverter system is modelled using the elements of Simulink. DC input voltage is shown in the Figure 7 and its value is 70V. The output voltage of the boost converter is shown in the Figure 8 and its value is 150V. The output voltage of the multilevel inverter is shown in the Figure 9. The peak value is 140V.

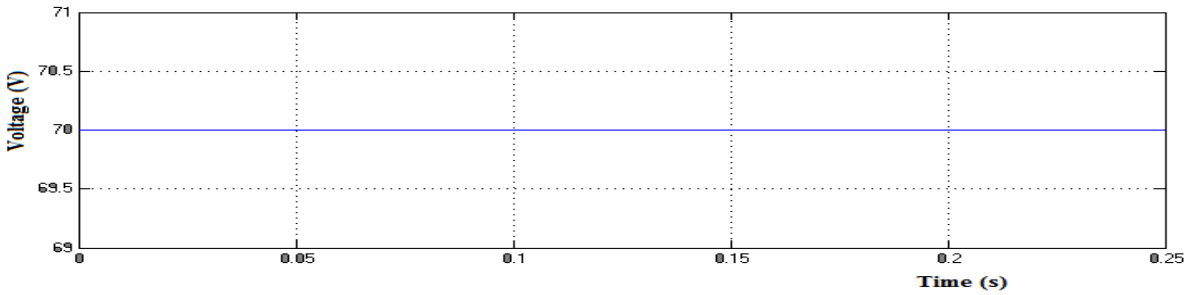

Figure: 7. Input voltage from PV pannel

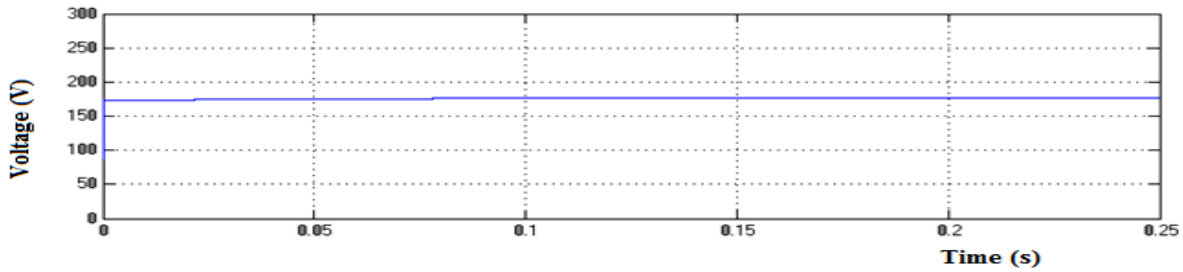

Figure: 8 Output voltage of the Boost converter

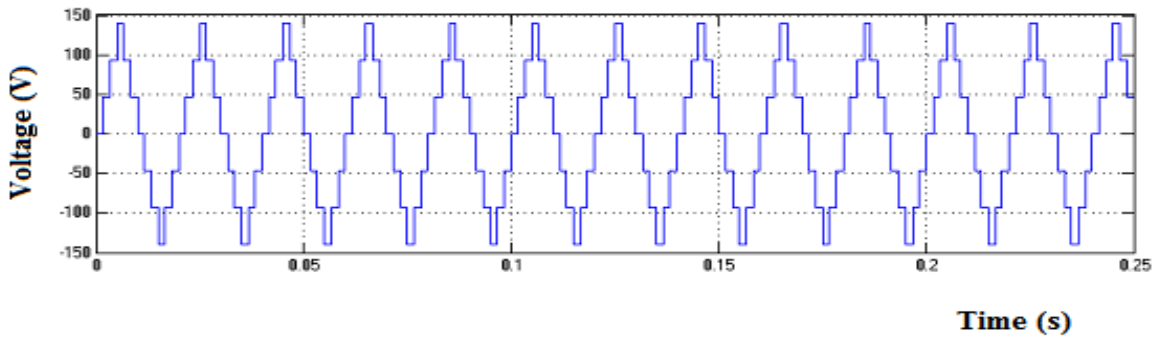

Figure: 9. Output voltage waveform of the multilevel inverter

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

Boost-SEPIC cascaded multi level inverter system is shown in Figure 10. The output of PV is stepped up in two stages using Boost and SEPIC converters. A single phase induction motor is used as the load. Output voltage of solar system is shown in Figure 11. Boost converter circuit and its input current ripple are shown in Figure 12 &13 respectively. The output voltage of the Boost converter is shown in Figure 14. SEPIC converter and its input current ripple are shown in Figure 15 & 16 respectively. The peak to peak ripple is 5A. The output voltage of SEPIC converter is shown in Figure 17 and its value is 100V.Switching pulses for M1 and M3 of MLI are shown in Figure18. The output voltage of MLI is shown in Figure 19. The peak value is 200V. The speed response is shown in Figure 20. The speed setteles at 1400RPM. The frequency spectrum for the output is shown in Figure 21 The THD is 16.7%. The comparison of Boost – Boost and Boost - SEPIC systems are given in Table 1. The comparison is done in terms of current ripple, output power and THD.

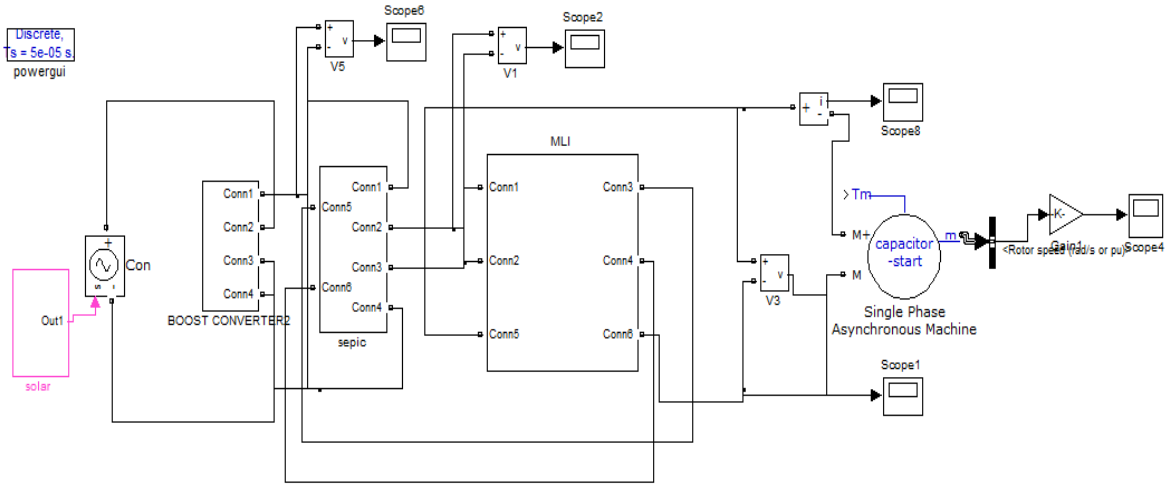

Figure: 10. Boost with SEPIC converter based MLI

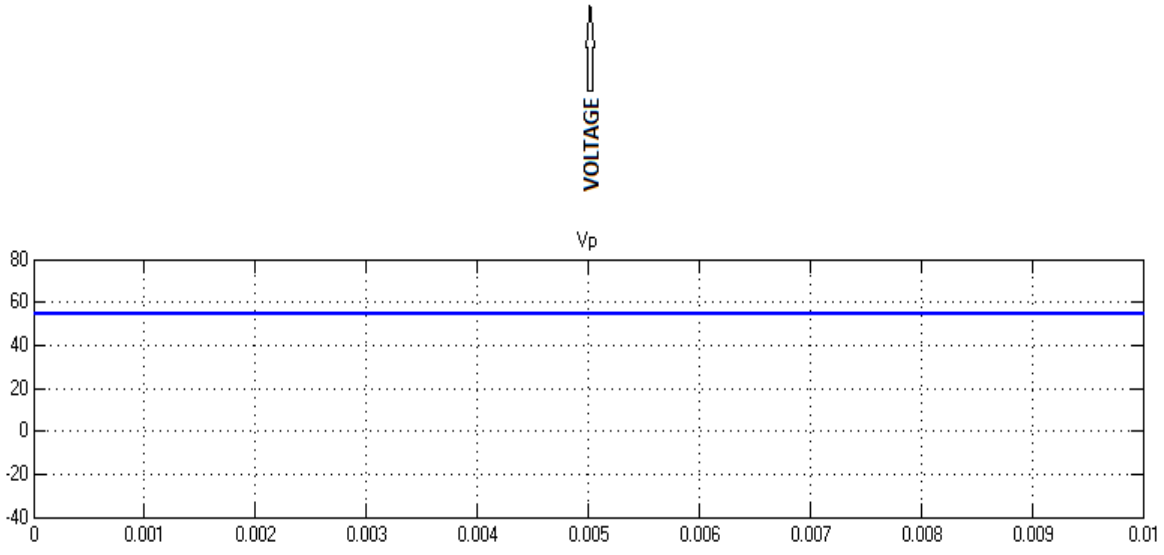

Figure: 11 PV output voltage

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

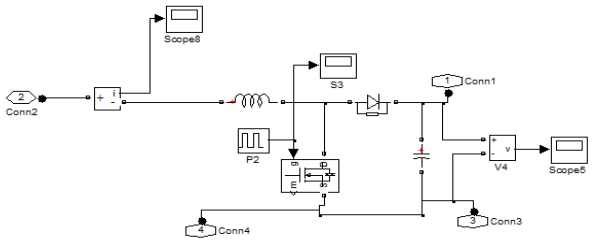

Figure: 12. Boost Converter Circuit

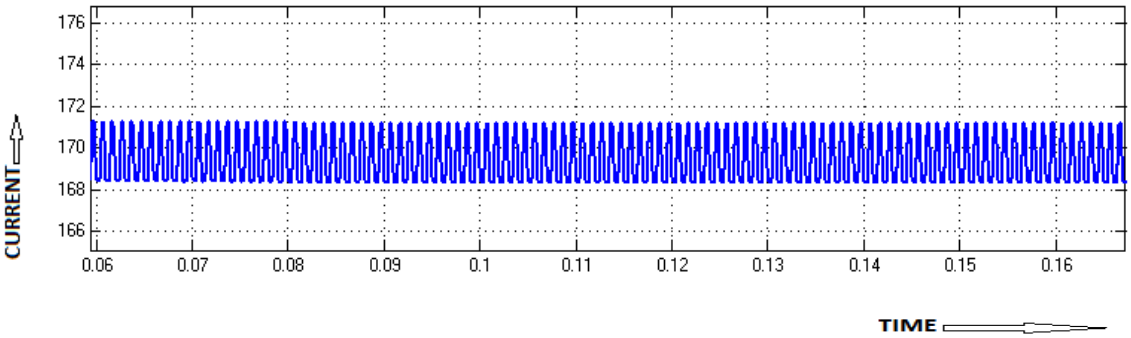

Figure: 13. Input current ripple of Boost converter

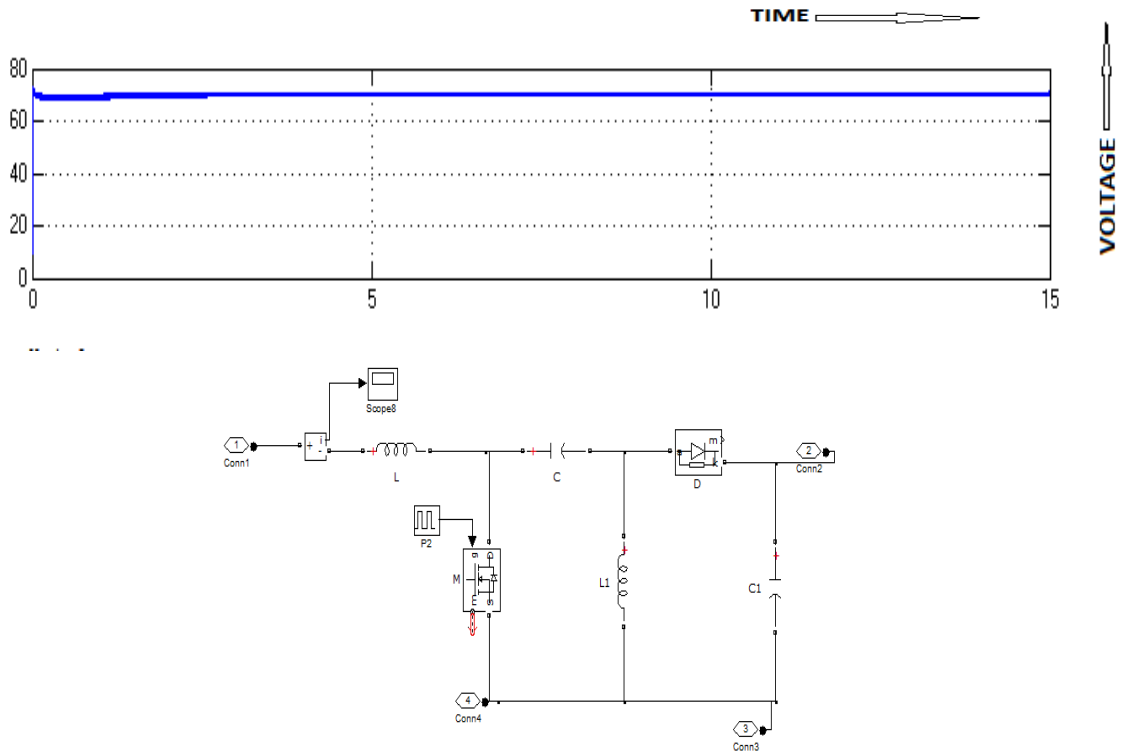

Figure: 15. SEPIC converter circuit

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

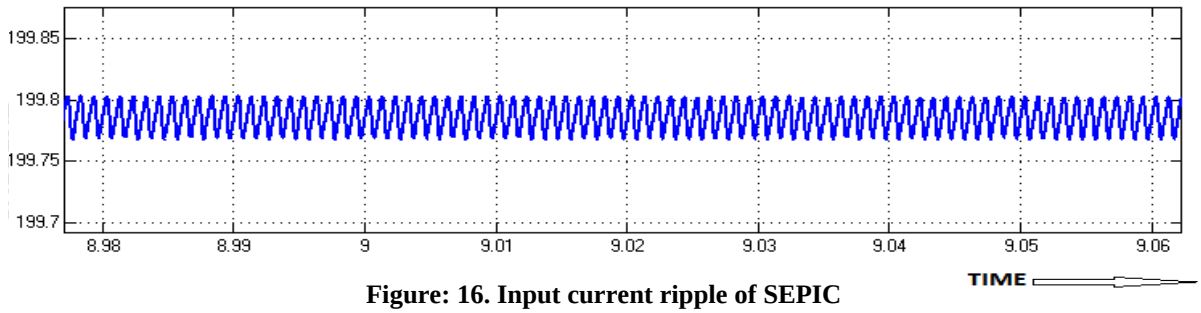

Figure: 16. Input current ripple of SEPIC

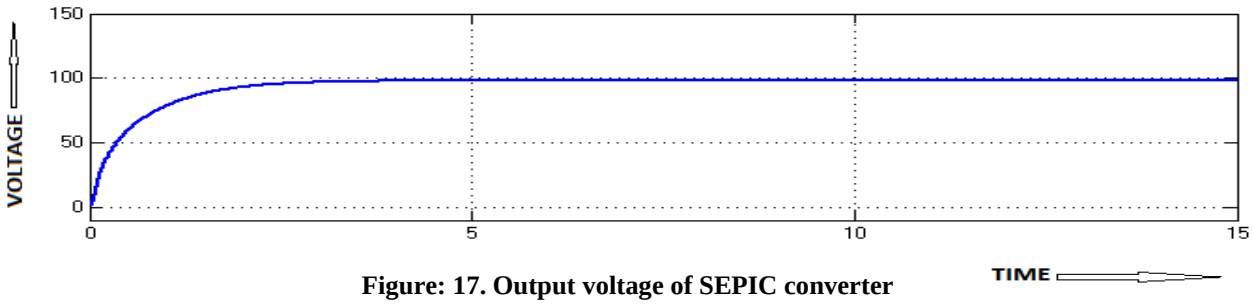

Figure: 17. Output voltage of SEPIC converter

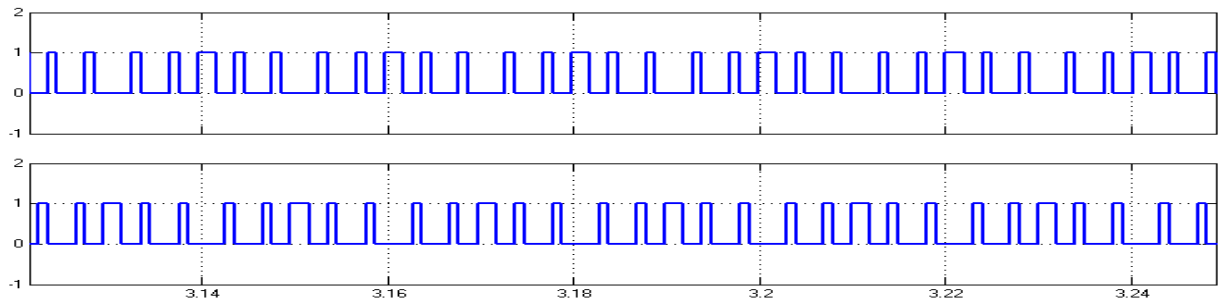

Figure: 18. Switching pulse for M1 & M3 of MLI

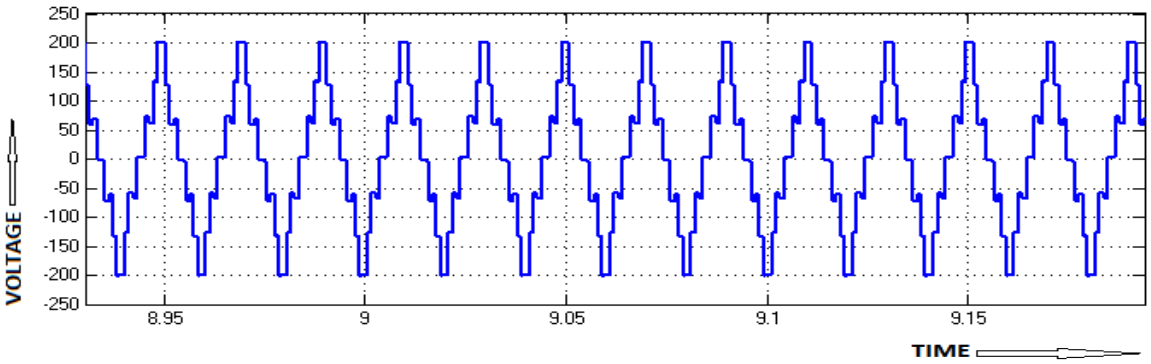

Figure: 19. Output voltage of multilevel inverter

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

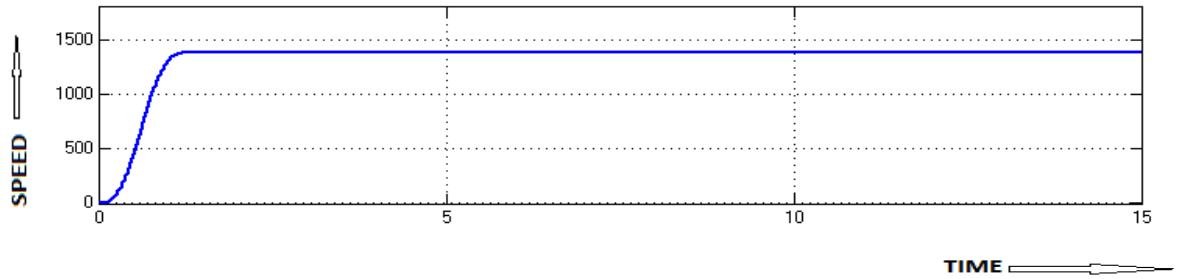

Figure: 20. Motor Speed

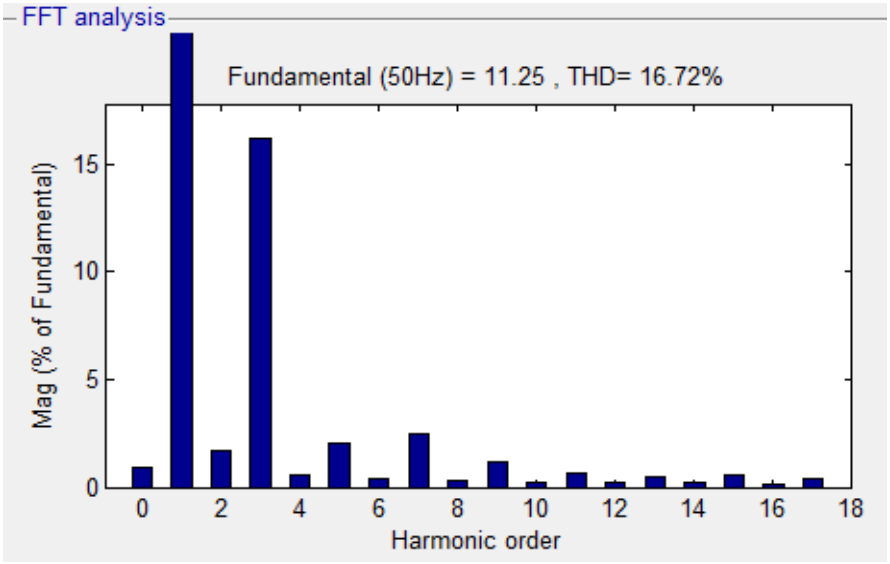

Figure: 21. Frequency Spectrum

Converter	Input Ripple Current	Power (Po)	THD %
Boost	3.5A	3125W	24.16%
SEPIC	0.04A	3320W	16.72%

Table 2: Comparison of Current ripple & Output Power

Controllers	Rise time (s)	Peak time (s)	Setting time (s)	Steady state error (V)
PI	3.3	3.4	4.2	2.3
FLC	0.4	0	0.5	1.4

Table 3 : Summary of responses with PI & FLC

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

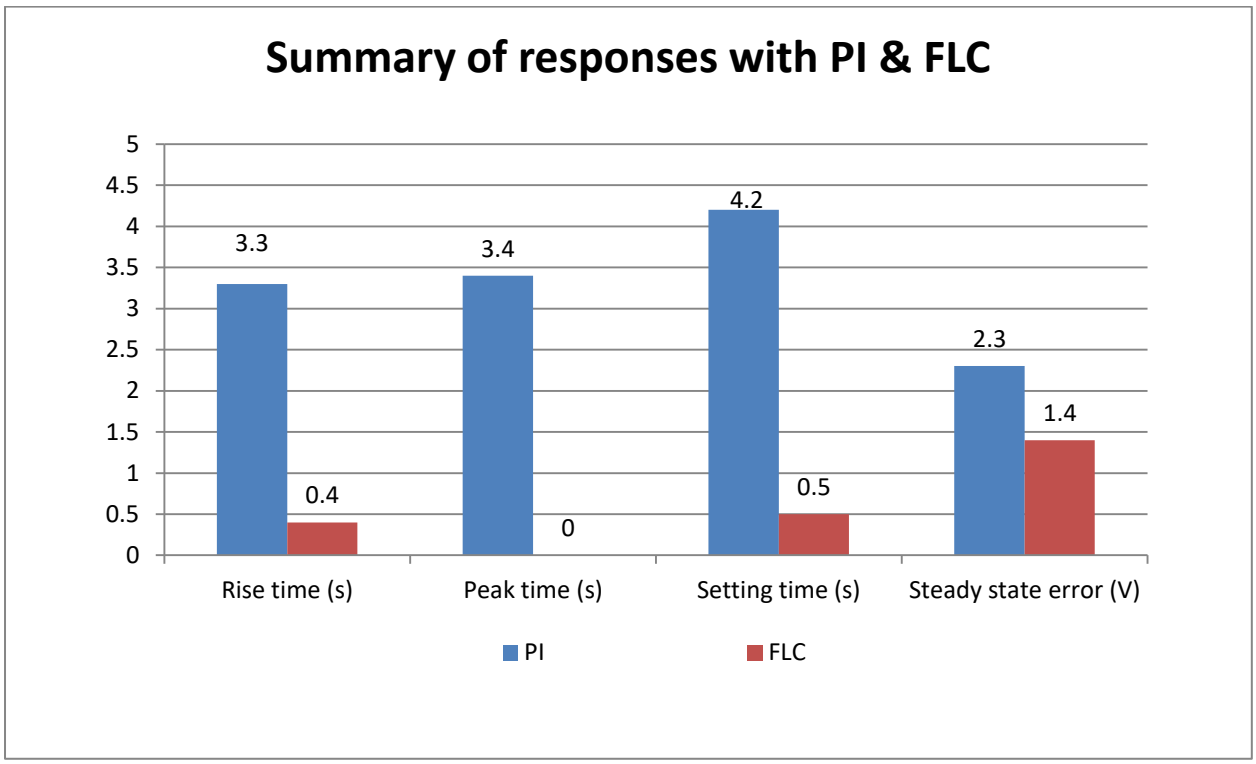

Figure: 22. Comparison chart of summary of response with PI & FLC

CONCLUSION:

The comparison indicates that boost to SEPIC converter for FLC based system is very smooth with negligible steady state error when compared to PI controlled system. The results indicate that the circuit generates seven level output with very low THD. The advantages of the proposed system are negligible settling time, negligible steady state error and reduced number of switches. The disadvantages of the system are that it requires two capacitors and coupled inductor. The scope of this work is the comparison of PI and FLC controller for boost to boost and boost to SEPIC converter based solar power generation system. From this analysis boost to SEPIC converter based FLC has more reliable than the boost to boost converter .

REFERENCES

[1] R. A. Mastromauro, M. Liserre, and A. Dell'Aquila, "Control issues in single-stage photovoltaic systems: MPPT, current and voltage control," *IEEE Trans. Ind. Informat.*, vol. 8, no. 2, pp. 241–254, May. 2012.

[2] Z. Zhao, M. Xu, Q. Chen, J. S. Jason Lai, and Y. H. Cho, "Derivation, anal- ysis, and implementation of a boost–buck converter-based high-efficiency pv inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1304–1313, Mar. 2012.

[3] M. Hanif, M. Basu, and K. Gaughan, "Understanding the operation of a Z-source inverter for photovoltaic application with a design example," *IET Power Electron.*, vol. 4, no. 3, pp. 278–287, 2011.

[4] J.-M. Shen, H. L. Jou, and J. C. Wu, "Novel transformer-less grid- connected power

converter with negative grounding for photovoltaic gen- eration system," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1818–1829, Apr. 2012.

[5] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics Converters, Applications and Design*, Media Enhanced 3rd ed. New York, NY, USA: Wiley, 2003.

[6] K. Hasegawa and H. Akagi, "Low-modulation-index operation of a five- level diode-clamped pwm inverter with a DC-voltage-balancing circuit for a motor drive," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3495–3505, Aug. 2012.

[7] E. Pouresmaeil, D. Montesinos-Miracle, and O. Gomis-Bellmunt, "Control scheme of three-level NPC inverter for integration of renewable energy resources into AC grid," *IEEE Syst. J.*, vol. 6, no. 2, pp. 242–253, Jun.2012.

[8] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalization in neutral clamped inverters for DSTATCOM application," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2768–2775, Aug. 2010.

[9] M. Chaves, E. Margato, J. F. Silva, and S. F. Pinto, "New approach in back-to-back m-level diodeclamped multilevel converter modelling and direct current bus voltages balancing," *IET power Electron.*, vol. 3, no. 4, pp. 578–589, 2010.

[10] J. D. Barros, J. F. A. Silva, and E. G. A Jesus, "Fast-predictive optimal control of NPC multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 60, no. 2, pp. 619–627, Feb. 2013.

[11] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multicell converter based on modified phase-shifted pulsewidth modulation," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1517–1526, Jun. 2010.

[12] S. Thielemans, A. Ruderman, B. Reznikov, and J. Melkebeek, "Improved natural balancing with modified phase-shifted PWM for single-leg five- level flying-capacitor converters," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1658–1667, Apr. 2012.

[13] S. Choi and M. Saeedifard, "Capacitor voltage balancing of flying capacitor multilevel converters by space vector PWM," *IEEE Trans. PowerDelivery*, vol. 27, no. 3, pp. 1154–1161, Jul. 2012.

[14] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade pwm converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1099–1107, Mar. 2012.

[15] X. She, A. Q. Huang, T. Zhao, and G. Wang, "Coupling effect reduction of a voltage-balancing controller in single-phase cascaded multilevel con- verters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3530–3543, Aug.2012.

[16] J. Chavarria, D. Biel, F. Guinjoan, C. Meza, and J. J. Negroni, "Energy- balance control of PV cascaded multilevel grid-connected inverters un- der level-shifted and phase-shifted PWMs," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 98–111, Jan. 2013.

[17] J. Pereda and J. Dixon, "High-frequency link: A solution for using only one DC source in asymmetric cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3884–3892, Sep. 2011.

[18] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electr.*, vol. 58, no. 6, pp. 2435–2443, Jun. 2011.

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 2 ISSUE 6 (2016) PAGES 1341 - 1354
RECEIVED : 29/10/2016. PUBLISHED: 16/11/2016
November 16, 2016

About Authors

D. Jasmine has done her B.E in Adhiyamaan College of Engineering, Hosur in the year 2005 & M.E in Madha Engineering College in the year 2011 respectively. She is presently a research scholar at St. Peters university, Chennai. Her research area includes Harmonic reduction in induction motor drives.

Dr. Gopinath Mani has obtained his B.E degree from Bharathiar University, Coimbatore in the year 2002. He obtained his M-Tech degree from Vellore Institute of Technology; Vellore in the year 2004.He obtained is Doctorate from Bharath University, Chennai in the year 2011. At present he is working as a Professor/EEE, at Dr.N.G.P Institute of Technology, Coimbatore, India. His Area of interest is Power Electronics.He is a professional member of IEEE, ISTE, IETE, IAENG, and IACSIT. He has received best performer award from GTEC in the year 2010. He also received VIDYA RATAN and Bharat Shiksha Ratan award from The Economic for Health & Educational growth in the years 2013& 2014 respectively.