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MULTIPLIERLESS HIGH PERFORMANCE FFT COMPUTATION

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Abstract:

A high performance hardware FFT have numerous application in instrumentation and communication systems. It describes new parallel FFT architecture which combines the split-radix algorithm with a constant geometry interconnect structure. The split-radix algorithm knows to have lower multiplicative complexity than both radix-2 as well as radix-4 algorithm. The split-radix algorithm maps onto a constant geometry interconnect structure in which the wiring in each FFT stage is indistinguishable, resulting in low multiplexing overhead. We are exploiting the lower arithmetic complexity of split-radix to lower dynamic energy, by gating the multipliers during trivial multiplication. The proposed FFT accomplishes less power than a parallel radix-4 design when computing at some point, the real-valued transform.

Key Words: FFT (Fast Fourier Transform), orthogonal frequency division multiplexing (OFDM), ultra-wideband (UWB).

1. INTRODUCTION

Discrete Fourier Transform generates a fixed duration discrete frequency sequence that is obtained by sampling one period of Fourier Transform. Fast algorithms for computing the DFT which are called as fast Fourier transform (FFT). FFT computes the DFT and produces accurately the same result as calculating the DFT definition directly. The dissimilarity is that an FFT is much faster. FFT is applicable in communications. The split-radix FFT has lower complication than the radix-4 or any higher-radix power-of-two FFT. In 2005, Y. W. Lin shows that the pipelined FFT architecture which is called as mixed-radix multipath delay feedback (MRMDF). The power consumption and hardware cost was also collect in this processor by using the higher radix FFT algorithm with less memory and complex multipliersA novel 128-point FFT/IFFT processor for OFDM-based UWB systems was proposed. In addition, the number of complex multiplications is less effectively reduced by using a higher radix algorithm [7]. In 2010 Shen-Jui Huang used the eight-data-path 2048-point FFT processor that has been proposed with a T.R. of 2.4 GS/s for OFDM-based gigabit WPAN application as well as consumed less power. Proposed work was based on split radix FFT architecture. FFT Computation can be done using different algorithm based on Radix 2, Radix 4, Radix 8, Split Radix etc. The split-radix algorithm has lesser multiplicative complexity than both radix-2 and radix-4 algorithms. The split-radix FFT mixes radix-2 and radix-4 decompositions. The split-radix FFT has lower complication than the radix-4 or any higher-radix power-of-two FFT.

2. FFT ARCHITECTURE

In the previous work author observe on the pipelined FFT architecture using more pipelines, consisting of logr N stages of butterfly data-paths. This paper describes parallel architecture with N/r

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butterfly data-paths. Fig.1 shows the structure of radix-2 and radix-4 butterfly. The N-point, radix-r complex valued FFT contains N/r logr N butterfly operations, therefore the throughput of an FFT architecture is limited by the number of butterfly operations computed in parallel. The row wise parallelization is used in pipelined FFTs, but it is doesn't impossible to parallelize along a column of the SFG. The N/r butterflies are instantiated to determine one stage means one column of the FFT. One column of registers is used to register the output. The split –radix algorithm provides the advantage of smaller amount of non- trivial complex multiplication and addition than radix-2, radix-4, and radix-8 algorithm. The split-radix algorithm is based on [3] succession decomposing in an N-point DFT into an N/2-point DFT and two N/4 –point DFTs. WkN=e-j2Πk/N, this is a twiddle factor used in FFT calculation. Using a pair of radix -2-like butterflies as the basic processing unit.

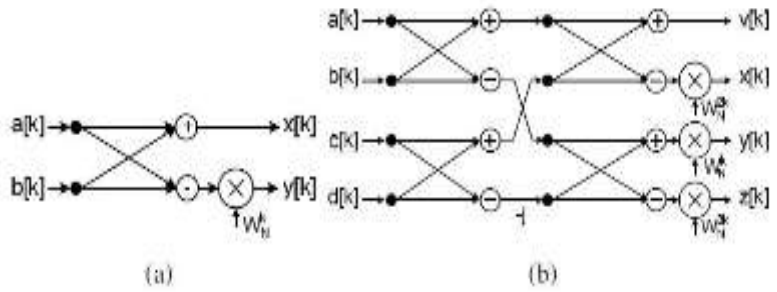

Fig.1.Block Diagram Of FFT Architecture

The split radix SFG thought of as a Cooley–Tukey radix-2 SFG, except with dissimilar twiddle factors and details in the butterflies. The split-radix SFG can be reschedule in the same way that a radix-2 Cooley–Tukey algorithm is changed into a constant geometry algorithm. The odd butterflies do not compulsory any multipliers, while the even butterflies necessitate two due to the presence of two twiddle factors. Thus referring to these butterflies as type 1 and type 2 butterflies vary from radix-2 butterflies in two main ways. First, when the butterfly is used to determine the second half of the 4-point DFT a subtraction occurs in the top branch rather than the bottom branch. Second, butterflies are modified to calculate multiplication by$\sqrt{-1}$ (j) without having to use the complex multiplier. This is particularly important in the split-radix design because the algorithm decreases the number of non-trivial multiplications at a cost of additional multiplications by j. These numbers of multiplications obtained only by non-trivial twiddle factors and by j.

3. PROPOSED METHOD

The proposed methodology are design n bit Adder for addition purpose, design n bit Multiplier for multiplication, design n bit complex multiplier is used to perform complex multiplication in FFT algorithm and also design n bit split radix butterfly for generate the butterfly structure, design reorder and the storing purpose design the register. In above show in the FFT architecture diagram .By the help of this diagram we design the code for floating point adder, floating point multiplier as well as One stage FFT. Also design the two stage FFT and Three stage FFT. And finally design code the Butterfly using split radix FFT. In the proposed methodology, at that time we work on the Adder and collect the output.

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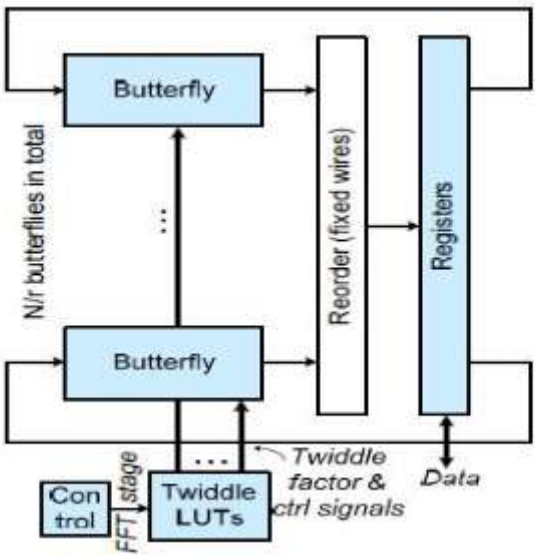

Fig.2. Proposed Architcture

4. MULTIPLIER GATING FOR SWITCHING POWER REDUCTION

The lesser multiplicative complexity of split-radix can be leveraged to reduce power. Specifically, trivial multiplications (i.e. multiplying by 1 or √–1). More importantly, during bypass, the multiplier inputs should be assumed that values from the previous cycle in order to suppress switching. At one multiplier input, this is done by putting in a latch. When the multiplier is bypassed, the latch holds data from the previous cycle, otherwise the latch is clear. Like the other control signals, the latch enable signals can be controlled via minute, hard-coded lookup tables. The latches can be build-up during timing verification by forcing the enable signal to "1", in which case they add a small delay to the logic path. The other multiplier input is controlled by tough-coded twiddle factor lookup tables. Therefore, we can modify the tables to replace "1" or " √ – 1" values with twiddle factor values from the previous cycle. The net result is that during trivial multiplications, the multiplier output remains unchanged from the previous cycle, but this incorrect output is bypassed.

5. CONSTANT MATRIX FFT

In the proposed FFT, a split –radix algorithm is a constant geometry interconnected structure. The profits of this structure are lower power, shorter critical path than radix-4 constant geometry architecture. The split –radix algorithm provides the advantage of smaller amount of non-trivial complex multiplication and addition than radix-2, radix-4, and radix-8 algorithm. The split-radix algorithm is based on [3] succession decomposing in an N-point DFT into an N/2-point DFT and two N/4 –point DFTs. WkN=e-j2Πk/N, this is a twiddle factor used in FFT calculation. Using a pair of radix -2-like butterflies as the basic processing unit. The split radix SFG thought of as a Cooley–Tukey radix-2 SFG, except with dissimilar twiddle factors and details in the butterflies. The split-radix SFG can be reschedule in the same way that a radix-2 Cooley–Tukey algorithm is changed into a constant geometry algorithm. The odd butterflies do not required any multipliers, while the even butterflies necessitate two due to the presence of two twiddle factors. Thus referring to these butterflies as type 1 and type 2 butterflies vary from radix-2 butterflies in two main ways. First, when the butterfly is used to determine the second half of the 4-point DFT a

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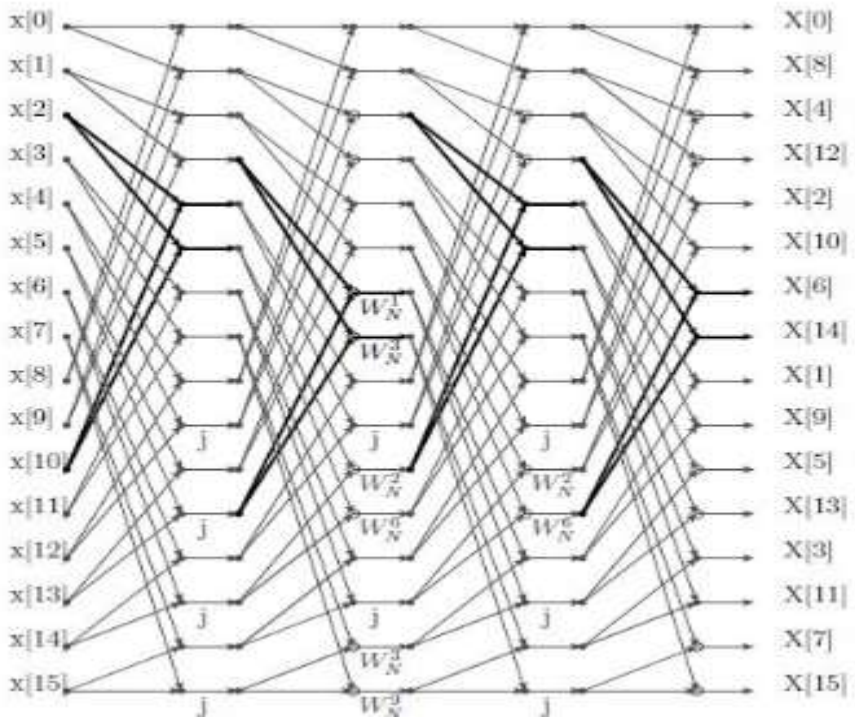

Fig.2. Rearrangement of a 16-point split-radix algorithm

subtraction occurs in the top branch rather than the bottom branch. Second, butterflies are modified to calculate multiplication by$\sqrt{-1}$ (j) without having to use the complex multiplier. This is particularly important in the split-radix design because the algorithm decreases the number of non-trivial multiplications at a cost of additional multiplications by j. These numbers of multiplications obtained only by non-trivial twiddle factors and by j.

CONCLUSION

N bit Adder is used to perform addition in FFT algorithm. CLA type of Adder is used in this design. Multiplier is used to perform real multiplication in FFT algorithm. Sequential type of multiplier has been used in these works. Complex multiplier is used to perform complex multiplication in FFT algorithm.Using the multiplier designed in the previous literatures split radix butterfly algorithm is realised. Because the split- radix algorithm is known to have lower multiplicative complexity than both radix-2 and radix-4 algorithms. It is used to generate the butterfly structure, like the upper and lower node calculations. For the reordering, the output purpose reorder block is used where reorder is register base. For output storing purpose register is used and Control block is used to control the overall system.

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