INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017

A TRANSFORMER-LESS DC VOLTAGE QUADRUPLER WITH LOW VOLTAGE STRESS FOR RENEWABLE SOURCE APPLICATION

Athira C R[1], Elangovan Devaraj[2]

[1]PG student, Dept. of Energy and Power Electronics, VIT University, Vellore
[2]Associate Professor, Dept. of Energy and Power Electronics, VIT University, Vellore
crathira@gmail.com

Abstract

This paper presents a transformer-less DC voltage quadrupler which is a DC-DC converter having boost topology. The system incorporates interleaving, high voltage transfer gain, input parallel and output series configuration and low voltage stress without any isolation. Interleaving helps in reducing the current handled by each switch through current sharing thereby reducing voltage and current rating of the switches, the switching as well as conduction losses. The clamping of voltage by the capacitors also helps in charge balance without introducing any complex circuitry. Also, the voltage stress of the switches and diodes is reduced considerably compared to other topologies. The paper covers modes of operation as well as steady state analysis of the proposed system along with a comparison table of the existing topologies. In the end, experimental results and simulation graphs are presented which emphasizes the efficiency and effective working of the converter.

Index Terms : Current sharing, Interleaving, Quadrupler.

1. INTRODUCTION

With global warming and solid natural developments, sustainable or clean vitality sources, for example, solar based cells and energy units are progressively esteemed around the world. In any case, because of the inherent natural low voltage of these sources, a high stride up dc converter is fundamental as a pre-stage of the relating power conditioner. The customary lift furthermore, buck–boost converters, because of the debasement in the generally speaking productivity as the obligation proportion approaches solidarity, clearly can't satisfy the application requirement. Additionally, the extraordinary obligation proportion not just instigates substantial voltage spikes and expands conduction misfortunes additionally prompts extreme diode reverse recovery issues. Numerous topologies have been displayed to give a high stride up voltage pick up without a to a great degree high obligation proportion as can be seen from the survey paper. A dc–dc fly-back converter is an exceptionally straightforward detached structure with a high venture up voltage pick up, yet the dynamic switch of this converter will endure a high voltage worry because of the leakage inductance of the transformer. For reusing the vitality of the leakage inductance also, limiting the voltage stress of the switch, a few methods have been proposed to reduce the voltage stress and to reuse the leakage inductance. Some isolated converters, for example, the phase shifted full-bridge converters, can accomplish a high stride up pick up by expanding the turns proportion of the transformer. Tragically, the higher current swell will lessen the most extreme yield control and abbreviate the

utilization life of electrolytic capacitor. To diminish the impacts, more electrolytic capacitors are required to stifle the extensive input current swell. Moreover, the resulting diode voltage stress is substantially higher than the output voltage, which will debase the circuit proficiency in high voltage applications. Other separated current-fed converters, for example, the active clamp dual boost converters and the active clamp full bridge boost converters, can understand high productivity and high stride up transformation. In any case, the start-up operation of these converters must be considered independently. In addition, the cost is expanded since numerous additional power segments and disengaged sensors or controllers are required. To decrease framework cost what's more, to enhance framework proficiency, a non-isolated dc-dc converter is, indeed, a more reasonable arrangement [6].

The clamped capacitor-based converters proposed in [14]–[16] give answers for enhance the transformation effectiveness what's more, accomplish expansive voltage change proportion. Tragically, the customary exchanged capacitor strategy makes the switch endure high transient currents and huge conduction losses. Moreover, many switched capacitor cells are required to get to a high degree voltage stride up , which builds the circuit multifaceted nature. Be that as it may, as of late a review on the efficiency of switched capacitor converters [13]; the creators exhibited some plan rules valuable for creating high-productivity switched capacitor converters, in view of their examination. In [24], a variety of converter topologies were exhibited in view of switched capacitor cell idea in which soft-switching was utilized to minimize switching loss and furthermore, electromagnetic interference [25], [26]. The coupled inductor-based converters are another arrangement to execute high gain in light of the fact that The turns proportion of the coupled inductor can be utilized as another control flexibility to broaden the voltage gain [11]–[18], [19]. In any case, the input current swell is generally bigger by utilizing single-stage coupled inductor-based converters, which may decrement the use life of the input electrolytic capacitor [9]. Considering this, a group of interleaved high step up boost converters with winding-cross-coupled inductors is proposed in [29]–[31], [20]. The passive lossless clamp or active clamp circuits are implemented to accomplish the soft-switching operation. On the other hand, some interleaved high step up converters with improved coupled inductors are acquainted with reduced circuit structure [12], [13], [22].

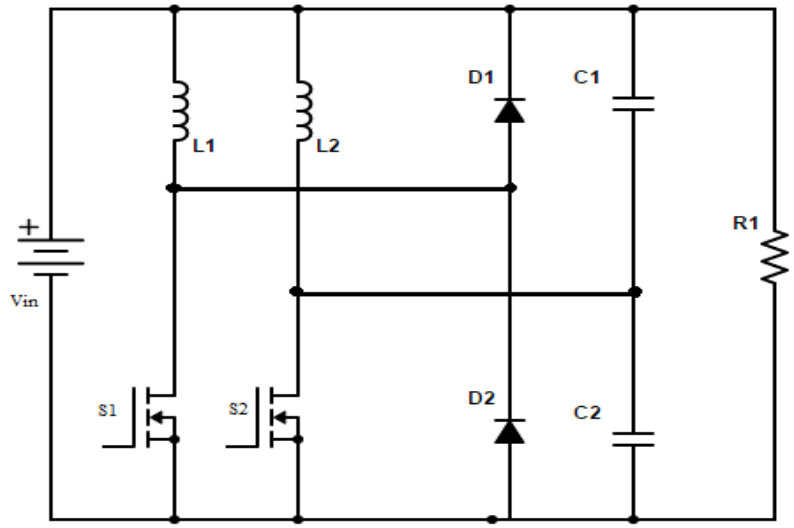
The interleaved voltage doubler [14] has been proposed for front end power factor correction with programmed current sharing ability and lower switch stress to increment the low-line effectiveness. Nonetheless, the voltage pick up is most certainly not sufficiently high and the diode voltage stress stays high [18]. To accomplish higher voltage conversion proportion and further diminish voltage weight on the switch and diode, the high step up proportion converter [15] and the ultrahigh step up converter [16] have been proposed. These converters can give substantial step up voltage change proportions. Sadly, the voltage stress of diodes in those converters remains rather high.

In this paper, a transformer-less flexible voltage quadrupler topology is proposed. It incorporates two-stage interleaved step up converter to attain a high voltage step up and keep up the benefit of current sharing ability at the same time. Moreover, the voltage stress of dynamic switches and diodes in the proposed converter can be enormously decreased to improve general output effectiveness. The rest of the substance of this paper might be laid out as takes after. To begin with, the circuit topology and operation guideline are given in Section II. At that point, comparing steady-state examination is made in Section III to give some fundamental converter qualities. A model is then built and some simulation outcomes are then introduced in Segment IV for showing the benefits and legitimacy of the proposed converter. At last, a few conclusions are offered in the last segment.

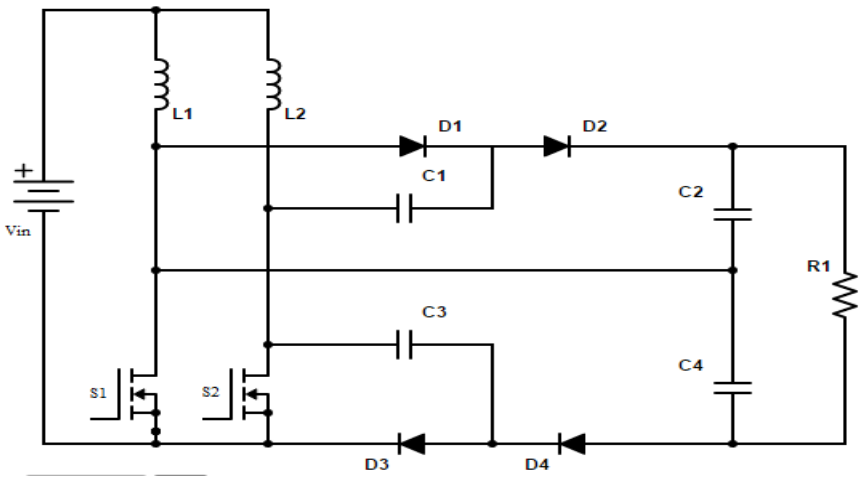
INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017

2. WORKING OF THE PROPOSED CONVERTER

For advantageous reference, the two-stage interleaved converter with parallel-input arrangement and series output association is first appeared in Fig. 1(a). The proposed converter topology is essentially gotten from a two-stage interleaved help converter and is appeared in Fig. 1(b). Looking at Fig. 1(a) with Fig. 1(b), one can see that two more capacitors and two more diodes are included so that the energy exchange is shared partially among one inductor and partially among another capacitor and inductor put vitality together to accomplish substantially higher voltage gain. In any case, the proposed voltage gain is twice that of the interleaved two-stage boost converter. Additionally, the voltage stress of both the dynamic switches and diodes are much lower in the proposed system compared to that of the existing system. Moreover, as will be clear last mentioned, the proposed converter



(a)



(b)

Fig 1 Circuit diagram of (a) existing converter (b) proposed converter

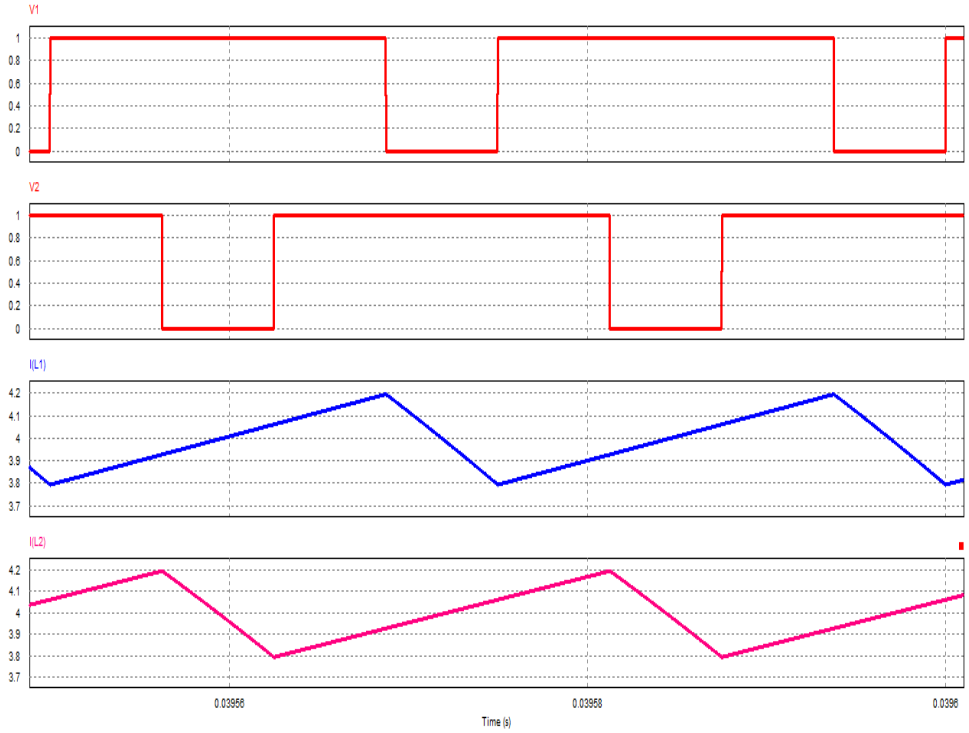
has uniform current sharing capacity without including additional hardware or, then again complex control techniques. The detailed working guideline can be represented as takes after.

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017

The proposed converter topology, similar to any current high stepup dc converter, has the disadvantage of presence of pulsating output period. Besides, as the fundamental target is to get high voltage gain and such trademark must be accomplished at the point when the duty cycle is more noteworthy than 0.5 and in continuous conduction mode (CCM); consequently, the steady state examination is made just for this case. Be that as it may, with duty cycle lower than 0.5 or in DCM, as there is no enough energy transfer from the inductors to the blocking capacitors, output capacitors, and load side, and subsequently it is unrealistic to get the high voltage gain as that for duty cycle more noteworthy than 0.5. Also, just with duty cycle bigger than 0.5, because of the charge balance of the blocking capacitor, the converter can highlight the inherent current sharing trademark that can hinder any additional current sharing control circuit. Then again, when obligation cycle is less than 0.5, the converter does not have the automatic current sharing capacity any more, and the current sharing control between each phases ought to be considered in this condition. Keeping in mind the end goal to simplify the circuit investigation of the proposed converter, a few assumptions are made as takes after.

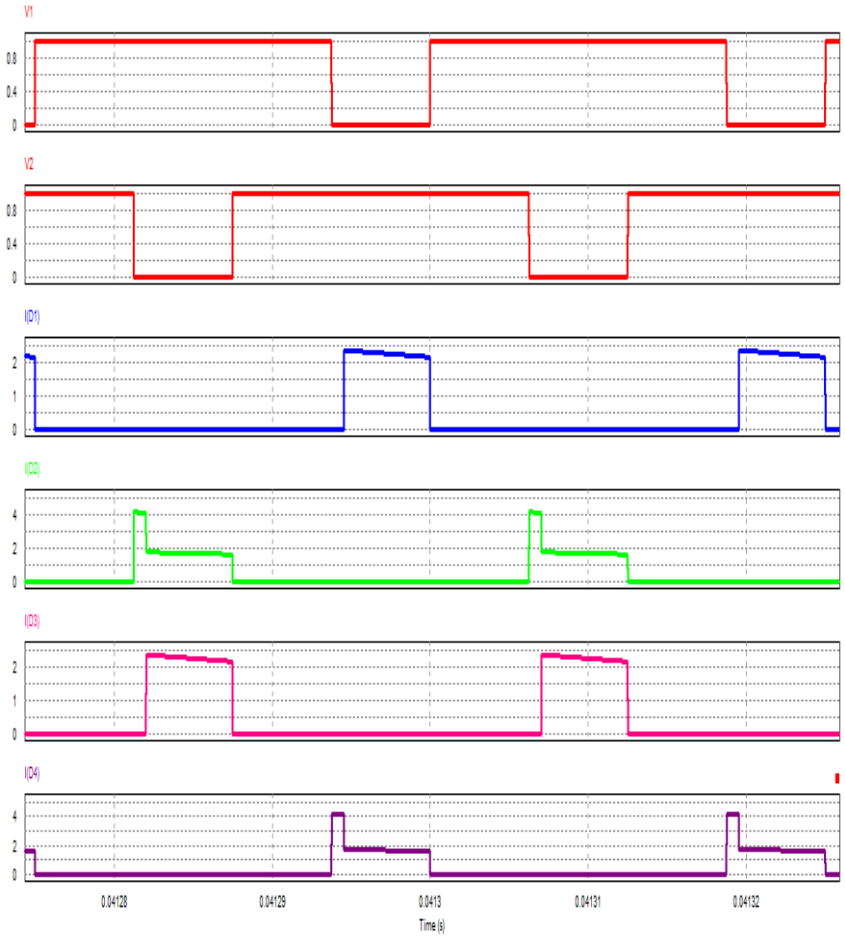
1) The components are ideal.
2) The capacitors are very large, to such an extent that the voltages across them are almost constant.
3) The framework is under steady state and is working in CCM also, with duty ratio being more prominent than 0.5 for high step up voltage.

Essentially, the working guideline of the proposed converter can divided into four operation modes. The interleaved gating signals with a 180^0 phase shift and waveforms are presented in Fig. 2.

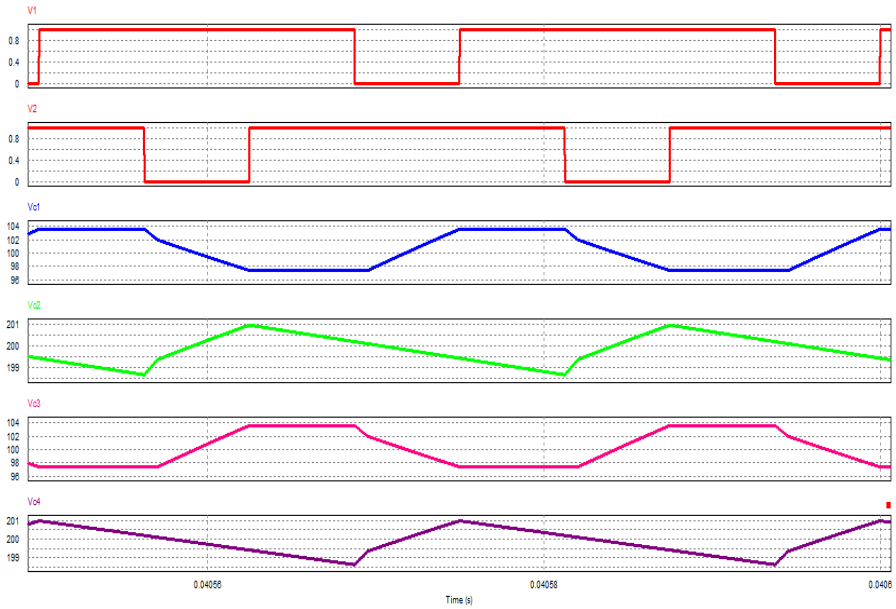


(a)

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017



(b)

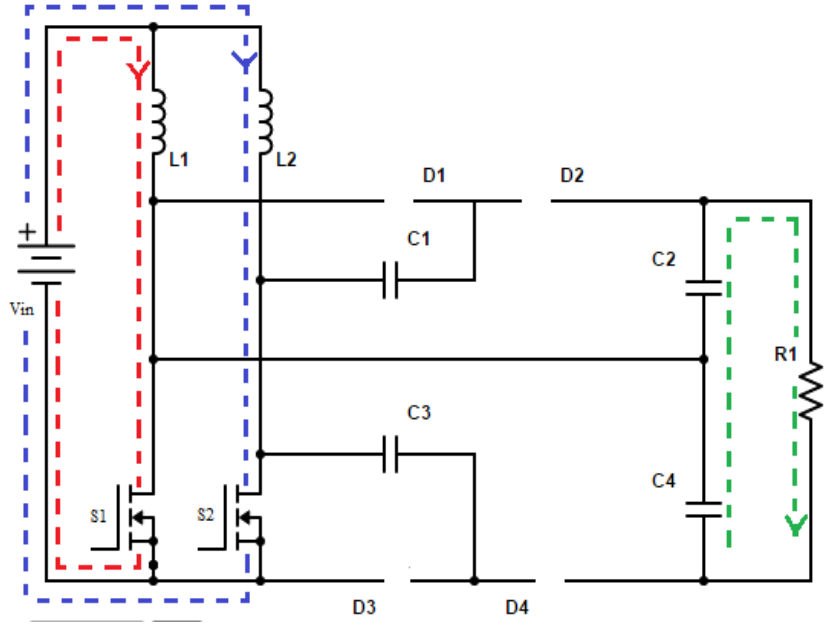


(c)

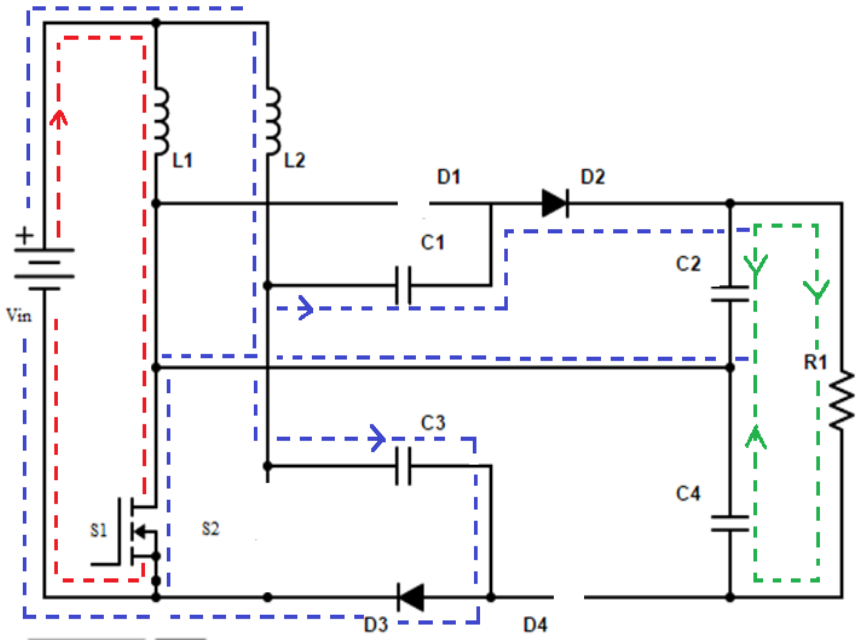
Fig. 2 (a) Inductor currents with respect to switching pulses (b) Diode currents with respect to switching pulses. (c)

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017

Capacitor charge and discharge.

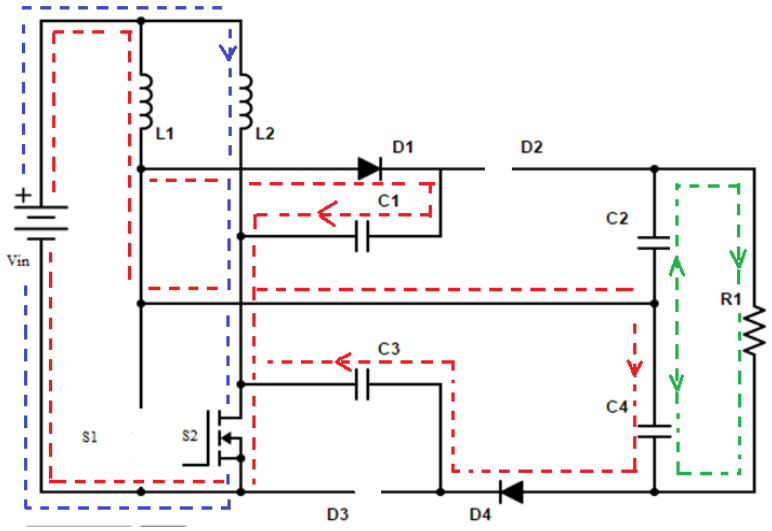


(a)



(b)

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017



(c)

Fig 3: Modes of operation. (a) Mode 1 and 3. (b) Mode 2. (c) Mode 4.

Mode 1: For mode 1, switches S1 and S2 are turned ON, diodes D1, D2, D3, D4 are all OFF. The corresponding equivalent circuit is shown in figure 3(a). Current passes through both the inductors and stores energy in them. The voltage across diodes D1 and D3 are clamped to capacitors C1 and C3 respectively, and the voltages across the diodes D2 and D4 are clamped to the voltage difference between the capacitors C1 and C2, and C4 and C3 repectively. C1 and C2 discharges to load. The corresponding equations are:

$L_1\ (diL1)/dt = V_i$

$L_2\ (diL2)/dt = V_i$

$C_1\ (dvc1)/dt = 0$

$C_3\ (dvc3)/dt = 0$

$C_4\ (dvc4)/dt = -\ (vc1 + vc2)/R$

$C_2\ (dvc2)/dt = -\ (vc1 + vc2)/R$

Mode 2: In this mode, switch S1 remains conducting and S2 is turned off. Diodes D2 and D3 remains conducting. The corresponding equivalent circuit is shown in figure 3(b). Part of energy stored in L2 and C1 is released to C2 and load. Other part of energy of L2 is stored in C3. The voltage across capacitor C2 is equal to the sum of voltages across capacitors C1 and C3. The corresponding equations are as follows:

$L_1\ (diL1)/dt = V_i$

$L_2\ (diL2)/dt = V_i + Vc1 - Vc2$

$C_1\ (dvc1)/dt = ic3 - iL2$

$C_3\ (dvc3)/dt = ic1 + iL2$

$C_4\ (dvc4)/dt = -\ (vc1 + vc2)/R$

$C_2\ (dvc2)/dt = -ic1 - (vc1 + vc2)/R$

Mode 3: The operation in this mode is similar to mode 1. Hence the equations are also same.

Mode 4: In this mode, switch S2 remains conducting and S1 is turned off. Diodes D1 and D4 remains conducting. The corresponding equivalent circuit is shown in fig 3(c). Part of energy in inductor L1 and that of capacitor C3 is

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017

released to C4 and load. The other part of energy stored in L1 is stored in C1. The voltage across capacitor C4 is equal

to the sum of voltages across capacitors C1 and C3. The corresponding equations are as follows:

$L_1\ (diL1)/dt = V_i$ - Vc4+Vc3

$L_2\ (diL2)/dt = V_i$

$C_1\ (dvc1)/dt = ic3 + iL1$

$C_3\ (dvc3)/dt = ic1 - iL1$

$C_4\ (dvc4)/dt = -ic3 - (vc1 + vc2)/R$

$C_2\ (dvc2)/dt = (vc1 + vc2)/R$

STEADY STATE ANALYSIS

VOLTAGE GAIN :

From mode 2,

$Vin - VL2 + VC1 - VC2 = 0$ (1)

$Vin - VL2 - VC3 = 0$ (2)

From (1) and (2)

$VC2 = VC1 + VC3$ (3)

From mode 4,

$Vin - VL1 - VC1 = 0$ (4)

$Vin - VL1 - VC4 + VC3 = 0$ (5)

From (4) and (5)

$VC4 = VC1 + VC3$ (6)

From mode 1 and mode 4,

$Vin\ D + (Vin - VC1\ )(1-D) = 0$ (7)

From mode 1 and mode 2,

$Vin\ D + (Vin - VC3\ )(1-D) = 0$ (8)

From (3),(6),(7) and (8),

$VC2 = VC1 + VC3 = (2Vin)/(1-D)$

$VC4 = VC1 + VC3 = (2Vin)/(1-D)$

$Vo = VC2 + VC4 = (4Vin)/(1-D)$

$Vo/Vin\ = 4/(1-D)$ (9)

VOLTAGE STRESS

From eqn. (7),

$Vc1 = 1/(1-D)\ Vin$

From mode 4,

$Vin - VL1 = VC1 = V(S1,max)$

$\therefore V(S1,max) = 1/(1-D)\ Vin$

From eqn. (9),

$Vo = 4/(1-D)\ Vin$

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017

$V(S1,max) = Vo/4$
From eqn. (8),
$Vc3 = 1/(1-D)\ Vin$
From mode 2,
$Vin - VL2 = VC3$
$\therefore V(S2,max) = 1/(1-D)\ Vin$
From eqn. (9),
$Vo = 4/(1-D)\ Vin$
$V(S1,max) = Vo/4$

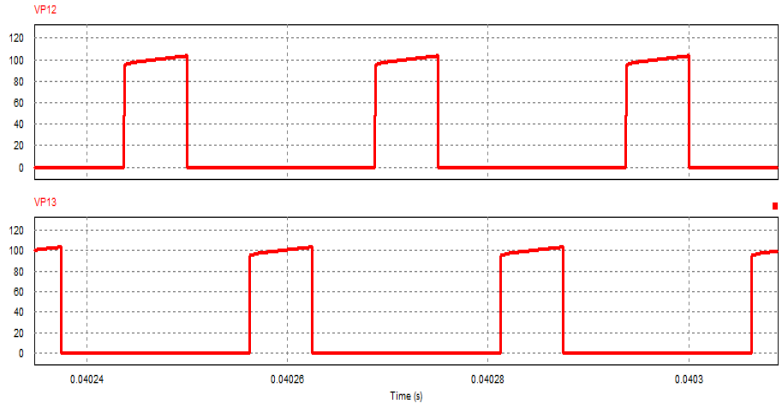


Fig 4 : Voltage across switches S1 and S2

From mode 1,
$V(D1,max) = VC1 = 1/(1-D)\ Vin$
$V(D2,max) = VC2 - VC1$
$= (2Vin)/(1-D) - Vin/(1-D)$
$= 1/(1-D)\ Vin$
$V(D3,max) = VC3 = 1/(1-D)\ Vin$
$V(D4,max) = VC4 - VC3$
$= (2Vin)/(1-D) - Vin/(1-D)$
$= Vin/(1-D)$
$V(D1,max) = V(D2,max) = V(D3,max) = V(D4,max)$
$= Vo/4$

DESIGN :
Vin = 25V
Vo = 400V
$f = 40KHz$
P = 200W
$R = Vo\text{^}2/P$ = 800Ω
$C1 = C3$ = 2μF
$C2 = C4$ = 4μF
Vo/Vin = $4/(1-D) \rightarrow 25/400 = 4/(1-D) \rightarrow D = 0.75$
$\Delta iL = (Vg\ D)/Lf$

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 2 (2017) PAGES 2043 - 2054
RECEIVED : 20.03.2017 PUBLISHED : 16.04.2017
April 16, 2017

ΔiL = 10% of iL
=10 % of $Vo/(R(1-D))$
= 10/100×400/(800(1−0.75))
= 0.2
L = $(Vg\ D)/(\Delta iL\ f)$
= (25×0.75)/(0.2×40000)
= 2344μH
$L1 = L2$ = 2344/2
= 1172μH each

Gain/stress	Voltage Doubler [24]	High step-up ratio converter [25]	Ultra high step-up converter [26]	Proposed converter
Voltage gain	$\frac{2}{(1-D)}$	$\frac{3-D}{(1-D)}$	$\frac{3+D}{(1-D)}$	$\frac{4}{(1-D)}$
Voltage stress of switches	$\frac{1}{2}$	$\frac{1}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{4}$
Voltage stress of diodes	1	$\frac{2}{(3-D)}$	$\frac{2}{(3+D)}$	$\frac{1}{2}$
numbers of MOSFETs	2	2	1	2
numbers of inductors	2	2	2	2
numbers of diodes	2	3	5	4
numbers of capacitors	2	3	4	4

TABLE.1. COMPARISON OF THE STEADY-STATE CHARACTERISTICS FOR FOUR CONVERTERS

3. SIMULATION RESULTS

The simulation is done in PSIM with 25 V input and and 400 V output. The duty ratio is 0.75 obtained from calculation and output power is 200 W. From figure 4, we can understand that the voltage across the switches is considerably reduced. Also, the voltage stress across the diodes are also reduced considerably.

CONCLUSION

In this paper, a novel transformer-less interleaved boost voltage quadrupler dc–dc converter with high voltage gain and decreased semiconductor voltage stress is proposed. The proposed topology uses input-parallel arrangement design and is gotten from a two-stage interleaved help converter for giving a considerably higher voltage pick up without receiving an outrageous huge duty cycle. The proposed converter can not only accomplish high voltage gain but also additionally lessen the voltage stress of both the dynamic switches as well as diodes. This will permit one to pick bring down voltage rating of MOSFETs and diodes to diminish both switching and conduction losses. What's more, due to the charge adjust of the blocking capacitor, the converter highlights

automatic uniform current sharing for the two interleaved stages in voltage boosting mode without including any additional hardware or complex control techniques. The operation rule what's more, relentless investigation and also a correlation with other late existing high stride up topologies are displayed. At long last, a 200-W rating model with 25-V input and 400-V yield is developed for checking the legitimacy of the proposed converter. It is seen that the subsequent test comes about to be sure concur close. Hence, the proposed converter is exceptionally appropriate for applications requiring high output voltage gain.

REFERENCES

[1] R. Erikson and D. Maksimovic, Fundamentals of Power Electroonics, Norwell, USA: Kluwer, 2001.
[2] Q. Zhao and F. C. Lee, "High-efficiency, high step-up DC–DC converters," IEEE Tranactions on Power Electronics, vol. 18, no. 1, pp. 65–73, Jan. 2013.
[3] N. P. Papanikolaou and E. C. Tatakis, "Active voltage clamp in flyback converters operating in CCM mode under wide load variation," IEEE Transactions on Industrial Electronics, vol. 51, no. 3, pp. 632–640, Jun. 2004.
[4] Q. Zhao, F. Tao, F. C. Lee, P. Xu, and J.Wei, "A simple and effective method to alleviate the rectifier reverse-recovery problem in continuous-current-mode boost converter," IEEE Transactions on Power Electronics, vol. 16, no. 5, pp. 649–658, Sep. 2001.
[5] W. Li and X. He, "Review of non-isolated high step-up DC/DC converters in photovoltaic grid-connected applications," IEEE Transactions on Industrial Electronics, vol. 58, no. 4, pp. 1239–1250, Apr. 2011.
[6] B. R. Lin and F. Y. Hsieh, "Soft-switching Zeta–Flyback converter with a buck–boost type of active clamp," IEEE Transactions on Industrial Electronics, vol. 54, no. 5, pp. 2813–2822, Oct. 2007.
[7] J. M. Kwon and B. H. Kwon, "High step-up active-clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems," IEEE Transactions on Power Electronics, vol. 24, no. 1, pp. 108–115, Jan. 2009.
[8] R. J. Wai, W. H. Wang, and C. Y. Lin, "High-performance stand-alone photovoltaic generation system," IEEE Transactions on Industrial Electronics, vol. 55, no. 1, pp. 240–250, Jan. 2008.
[9] C. M. Wang, "A novel ZCS-PWM flyback converter with a simple ZCS PWM commutation cell," IEEE Transactions on Industrial Electronics, vol. 55, no. 2, pp. 749–757, Feb. 2008.
[10] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC–DC converter for bidirectional high power applications," IEEE Transactions on Power Electronics, vol. 21, no. 2, pp. 422–429, Mar. 2006.
[11] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "Voltage multiplier cells applied to non-isolated DC–DC converters," IEEE Tranactions on Power Electronics, vol. 23, no. 2, pp. 871–887, Mar. 2008.
[12] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio," IEEE Transactions on Circuit Systems I, vol. 55, no. 4, pp. 1159–1171, May 2008.
[13] R. J. Wai and W. H. Wang, "Grid-connected photovoltaic generation system," IEEE Transactions on Circuit Systems I, vol. 55, no. 3, pp. 953–964, Apr. 2008.
[14] F. Zhang, L. Du, F. Z. Peng, and Z. Qian, "A new design method for high power high-efficiency switched-capacitor DC–DC converters," IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 832–840, Mar. 2008.

[15] L. S. Yang, T. J. Liang, H. C. Lee, and J. F. Chen, "Novel high step-up DC–DC converter with coupled-inductor and voltage-doubler circuits," IEEE Transactions on Industrial Electronics, vol. 58, no. 9, pp. 4196–4206, Sep. 2011.

[16] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/switched-inductor structures for getting transformerless hybrid DC–DC PWM converters," IEEE Transactions on Circuit Systems, vol. 55,no. 2, pp. 687–696, Mar. 2008.