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An hybrid design of high speed carry skip adder using AOI ana OAI techniques

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Abstract:

In this, we present a Carry-skip adder (CSKA) (another name for it is called as carry-bypass adder) is an adder implementation which helps on the delay of a ripple-carry adder with less effort when it is compared with rest of other adders. The accepted or followed structure of the CSKA consist the different stages containing chain relation of full adders (FAs) (RCA block) and 2:1 multiplexer. The RCA blocks are connected one to one by 2:1 multiplexers, which we can place in further level structures. Here we are presenting a method based on AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates logic is used to replace the MUX logic being used in traditional design. The presented methodology is about the comparison of power, energy and delay parameters with other existing adders. The concentration on the static CMOS originates from the desire to have are liably operating circuit under a wide range of supply voltages in highly scaled technologies. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented.

Keywords: Carry Skip Adder (CSKA), Energy Efficient, High Performance, Hybrid Variable Latency Adders, Voltage Scaling.

1. INTRODUCTION

Adders are a key building block in arithmetic and logic units (ALUs) [1] and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in . Obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage. Moreover, the subthreshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through the drain- induced barrier lowering effect. Depending on the amount of the supply voltage reduction, the operation of ON devices may reside in the superthreshold, near-threshold, or subthreshold regions. Working in the superthreshold region provides us with lower delay and higher switching and leakage powers compared with the near/subthreshold regions. In the subthreshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nanoscale

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technologies. The variations increase uncertainties in the aforesaid performance parameters. In addition, the small subthreshold current causes a large delay for the circuits operating in the subthreshold region.

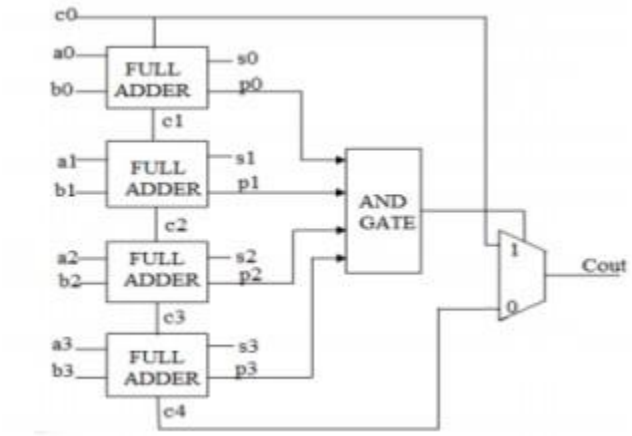

Fig.1. Four bit skip adder

The dependence of the power (and performance) on the supply voltage has been the motivation for design of circuits with the feature of dynamic voltage and frequency scaling. In these circuits, to reduce the energy consumption, the system may change the voltage (and frequency) of the circuit based on the workload requirement. For these systems, the circuit should be able to operate under a wide range of supply voltage levels. Of course, achieving higher speeds at lower supply voltages for the computational blocks, with the adder as one the main components, could be crucial in the design of high-speed, yet energy efficient, processors.

2. RELATED WORK

In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented.

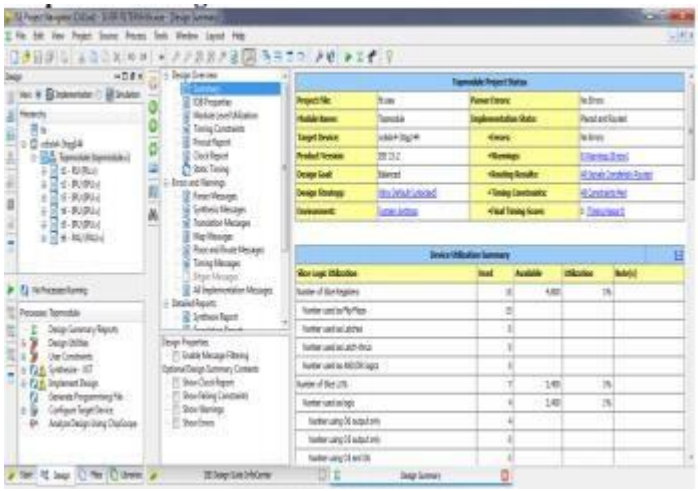

Fig.2. Design method

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To the best of our knowledge, no work concentrating on design of CSKAs operating from the super threshold region down to near-threshold region and also, the design of (hybrid) variable latency CSKA structures have been reported in the literature. In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic. The concentration on the static CMOS originates from the desire to have are liably operating circuit under a wide range of supply voltages in highly scaled technologies. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the super threshold region down to near-threshold region and also, the design of(hybrid) variable latency CSKA structures have been reported in the literature.

3. ANALYSIS

Proposing a modified CSKA structure by combining the concatenation and the incrementation schemes to the conventional CSKA (Conv-CSKA) structure for enhancing the speed and energy efficiency of the adder. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer.

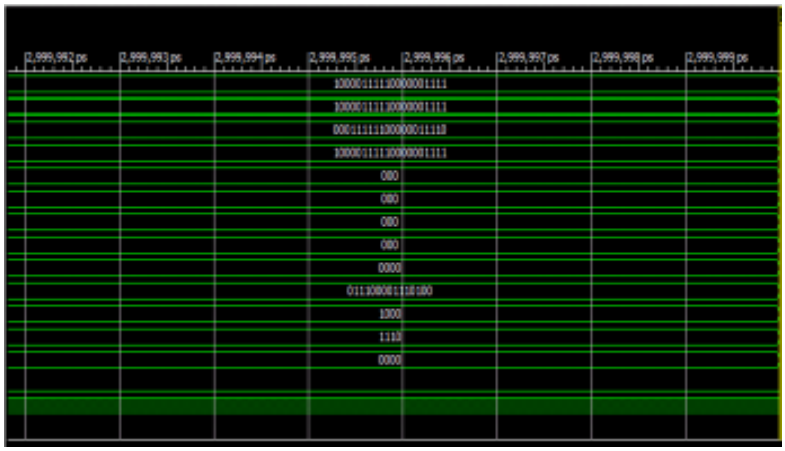

Fig.3. Generating values

Providing a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay. Investigating the impact of voltage scaling on the efficiency of the proposed CSKA structure(from the nominal supply voltage to the near-threshold voltage).Proposing a hybrid variable latency CSKA structure based on the extension of the suggested CSKA, by replacing some of the middle stages in its structure with a PPA, which is modified in this paper. There is to this paper is organized as follows. related work on modifying the CSKA structure for improving the speed as well as prior work that use variable latency structures for increasing the efficiency of adders at low supply voltages. the Conv-CSKA with fixed stage size (FSS) and variable stage size (VSS) is explained, while describes the proposed static CSKA structure. The hybrid variable latency CSKA structure is suggested.

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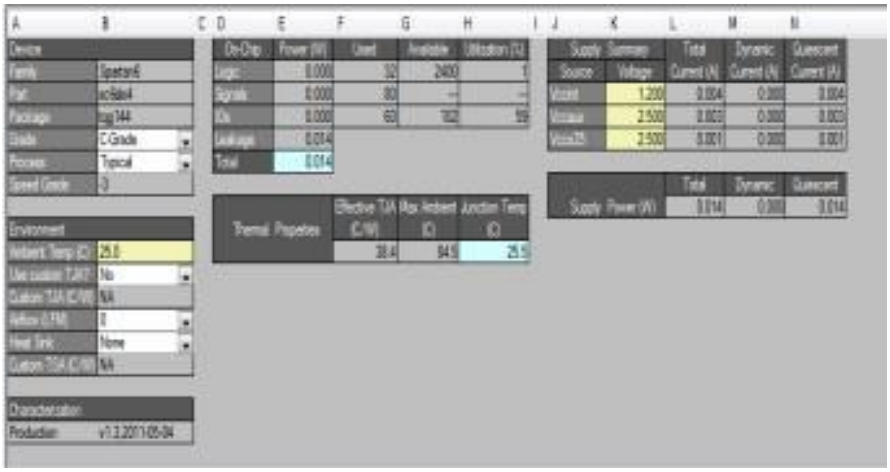

Fig.4. Power analysis

The RCA blocks are connected to each other through 2:1 multiplexers, which can be placed into one or more level structures. Many methods have been suggested for finding the optimum number of the FAs. The techniques presented in make use of VSSs to minimize the delay of adders based on a single level carry skip logic., some methods to increase the speed of the multilevel CSKAs are proposed. The techniques, however, cause area and power increase considerably and less regular layout. In addition, to lower the propagation delay of the adder, in each stage, the carry look-ahead logics were utilized. Again, it had a complex layout as well as large power consumption and area usage. In addition, the design approach, which was presented only for the 32-bit adder, was not general to be applied for structures with different bits lengths. Based on the discussion presented above, it is concluded that by reducing the delay of the skip logic, one may lower the propagation delay of the CSKA significantly.

CONCLUSION

In this paper, a static CMOS CSKA structure called CI- CSKA was proposed, which exhibits a higher speed and lower energy consumption compared with those of the conventional one. The speed enhancement was achieved by modifying the structure through the concatenation and incrementation techniques. In addition, AOI and OAI compound gates were exploited for the carry skip logics. The efficiency of the proposed structure for both FSS and VSS was studied by comparing its power and delay with those of the Conv-CSKA, RCA, CIA, SQRT-CSLA, and KSA structures. The results revealed considerably lower PDP for the VSS implementation of the CI-CSKA structure over a wide range of voltage. The results also suggested the CI-CSKA structure as a very good adder for the applications where both the speed and energy consumption are critical. In addition, a hybrid variable latency extension of the structure was proposed. The suggested structure showed the lowest delay and PDP making itself as a better candidate for high-speed low-energy applications.

REFERENCES

[1] I. Koren, Computer Arithmetic Algorithms, 2nd ed. Natick, MA, USA: A K Peters, Ltd., 2002.

[2] R. Zlatanovici, S. Kao, and B. Nikolic, ―Energy–delay optimization of 64-bit carry-lookahead adders with a 240 ps 90 nm CMOS design example,‖ IEEE J. Solid-State Circuits, vol. 44, no. 2, pp. 569–583, Feb. 2009.
[3] S. K. Mathew, M. A. Anders, B. Bloechel, T. Nguyen, R. K. Krishnamurthy, and S. Borkar, ―A 4-GHz 300-mW 64-bit integer execution ALU with dual supply voltages in 90-nm CMOS,‖ IEEE J. Solid-State Circuits, vol. 40, no. 1, pp. 44–51, Jan. 2005.
[4] V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, and R.Krishnamurthy, ―Comparison of high-performance VLSI adders in the energy-delay space,‖ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 754–758, Jun. 2005.
[5] B. Ramkumar and H. M. Kittur, ―Low-power and area- efficient carry select adder,‖ IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 371–375, Feb. 2012.
[6] M. Vratonjic, B. R. Zeydel, and V. G. Oklobdzija, ―Low- and ultra low-power arithmetic units: Design and comparison,‖ in Proc. IEEE Int. Conf. Comput. Design, VLSI Comput. Process. (ICCD), Oct. 2005, pp. 249–252.
[7] C. Nagendra, M. J. Irwin, and R. M. Owens, ―Area-time-power tradeoffs in parallel adders,‖ IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 43, no. 10, pp. 689–702, Oct. 1996.