INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2432 - 2436
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

A Novel Realization and Synthesis of TCAM Design Using Reversible Circuits

[1]B.Dhana Lakshmi, [2]Maddana,

[1]PG Scholar, Dept of VLSI System Design, Geetanjali college of engineering & technology,
[2]HOD Dept of ECE, Geetanjali college of engineering & technology.

Abstract:

CAM is the one of the special type of memory which is used to search the contents stored in the memory using the contents. Ternary content addressable memory is a memory which has three states logic 1, logic0 and logic x where search operation is performed within the single clock cycle. This memory component is designed using the reversible logic gates. Content addressable memory is a special type of memory which can do search operation in a single clock cycle. CAM has disadvantages of high power dissipation during the matching operation. Ternary content addressable memory (TCAM) is a special type of memory which is used to search for logic 0, logic 1, logic 'x'. These types of memory are used in routers in order to perform the lookup table function in a single clock cycle.

KeyWords: TCAM, Garbage output, Quantum cost, Power consumption.

1. INTRODUCTION

Ternary content Addressable memory is a one of the Special type of memory ,these memory has the three logic states ie: Logic "0", Logic "1" and Logic" x" this is used to perform the search operation within the Single Clock Cycle. TCAM finds the application in various fields. The main application of TCAM is found in the Network Routers where searching operation is done using the Contents. The other applications of the TCAM are found in Intrusion Detect, image processing, Gene pattern searching bioinformatics. The proposed concept is designed using the reversible logic gate. In Reversible logic gates, each and every computed information is stored, because of that there is no loss of data and loss of power. There are equal number of inputs and outputs in reversible gates and the information is reused in the circuit by avoiding the loss of information by not computing the information computed before. There are three factors in the reversible logic, Quantum cost, worst case Delay and Garbage outputs. There are few gates proposed namely Toffoli Gate which has the quantum cost of 5 which has 3 inputs and 3 outputs and Feyman gate has quantum cost of 1 and has two inputs and two outputs similarly many reversible gates have been proposed satisfying all the reversible properties. RAM needs an address to fetch the data stored in the memory whereas CAM needs the contents to be searched in the search lines and the matched address is obtained at the output. CAM is known for its high speed search operation. However, the CAMs consume lot of power due to its high speed operation and lot of heat is dissipated. High power consumption in CAM devices increases the junction temperatures of the chip which increases the heat dissipation there by reducing the performance of the chip [1].

In the conventional TCAM design, 16 transistors are used to do the search and match operations. The change in state of the transistors due to the changes in the bit of search line and match- line will lead to the heat dissipation of the circuits. It has been shown that the power consumption for the conventional 16T TCAM cell is approximately 12mW to 15mW of power [5]. This paper aims at presenting a novel TCAM

design using reversible elements as an alternate to reduce the power consumption in the TCAM cell. A novel SRAM cell is designed using the reversible elements which are used to store the data. The match line and the search line are also designed using reversible elements which emulate the conventional NAND type TCAM cell. To the best of our knowledge, this is the first paper on designing a novel TCAM cell using reversible elements. The design is verified by using Xilinx ISE simulator.

2. RELATED WORK

Content addressable memory is of two types based on the types of bits stored in it. Each and every CAM cells will have their own comparison and search circuitry in order to search and gives the address of the matched data. Binary CAM can store logic ’0’ and logic ’1’ whereas ternary CAM can store logic ’0’, logic ’1’ and don’t care.

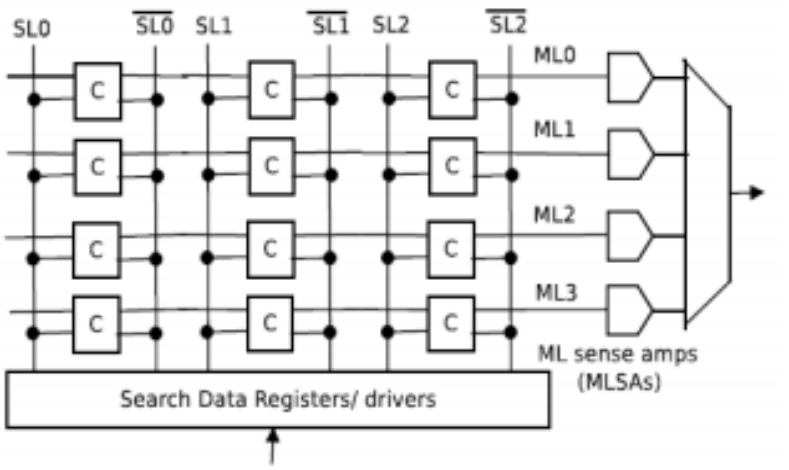

Fig.1. Conventional System

Thus in TCAM, the stored key 11x can match any one of the search keys of 110 or 111. TCAM cells are arranged in the 2D array format. The cells in the same row are connected through the common match-line and the cells in the column have common search-line. There are 3 stages in the conventional TCAM cell. Search line (SL) precharge, matchline (ML) precharge, match-line (ML) evaluate. During the search-line precharge operation, the search-line will be made high in order to disconnect the TCAM cells from the pull down path. In the next stage, that is during match-line precharge, the match-line will be charged high and in the last stage of the operation the matchline will be evaluate by placing the search bits in the search lines. If the data are matched then the matchline will be in high state else the match line state will discharge through the pull down path which proves the irreversibility operation of the TCAM cells.

3. IMPLEMENTATION

In this section we are going to discuss about the SRAM using reversible logic gates and about the conventional TCAM realized using the Conventional logic gates. Figure 6 shows the realization of the SRAM using reversible logic gates. Here in proposed design we use 3x3 Fredkin gate and 2x2 Feyman gate to realize the SRAM. This SRAM has the capacity to store single bit of data in it. SRAM has two states Hold state and Read/Write State. The operating modes of the SRAM Depends upon the WL when WL=0

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2432 - 2436
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

SRAM operates in Hold State and When WL=1 SRAM operates in Read/ Write Mode. Conventional TCAM. it consists of Two back inverted inverters connected to each other in opposite direction which acts as a memory to store a data it consists of SL and SL_bar which are known as search lines which are used to search the bit stored in the memory and ML(match line) which is output of the TCAM.

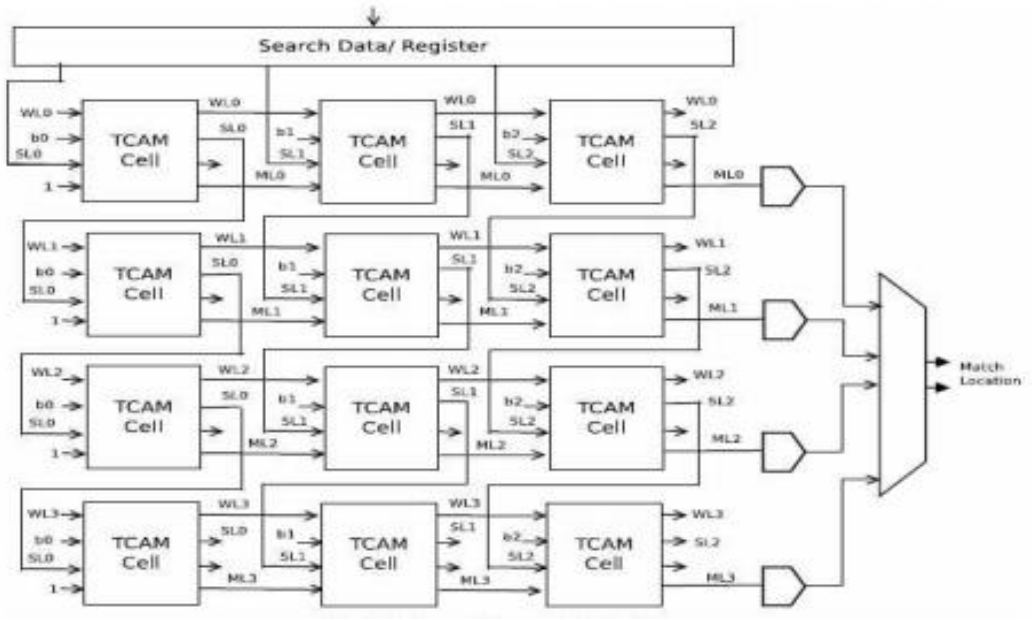

Fig.2. Proposed Analysis

In this part we discuss about the Single bit TCAM Realized Using the Reversible Logic gates. The Input data is given from the SRAM to the TCAM cell as a input to Feyman gate which is then connected to Feyman gate and then connected to the Fredkin gate the exored results is given as input to the to peres gate where output is obtained at Match line(ML) the same TCAM can be Realized by replacing the Peres gate by Tofoli gate .But the quantum cost of the Second design increases slightly which also effects the worst case delay of the circuit also but garbage outputs remain same for the both the design. This section discusses about the operation of TCAM array and how the data are searched and matched. So the output of the ex-or operation is 0. Whenever the data are matched the output of the ex-or operation is 0 which is then inverted to get the output 1. This resembles the functionality of the conventional binary CAM cell. The data stored in the TCAM is either logic '0'/logic '1' or don't care bit based on the value of the match bit.

4. SIMULATION ANALYSIS

Reversible Logic gates are nothing but the gates having the same number of inputs as well as same number of outputs. Where the inputs and outputs of the gate are mapped with each other. There are 3 factors related to the reversible logic gates, Quantum cost, Worst case delay and garbage outputs. Feyman gate which is said to be controlled Not gate having two inputs and two outputs which is said to be 2x2 and having the quantum cost of 1with worst case delay of 1. Fredkin gate is 3x3 reversible gate having the quantum cost of 5 and worst case delay of 5. Tofoli gate is 3x3 one of the reversible gate having the quantum

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2432 - 2436
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

cost of 6 with worst case delay of 6.peres gate is also 3x3 the member of reversible logic gate family with quantum cost of 4 with worst case delay of 4.

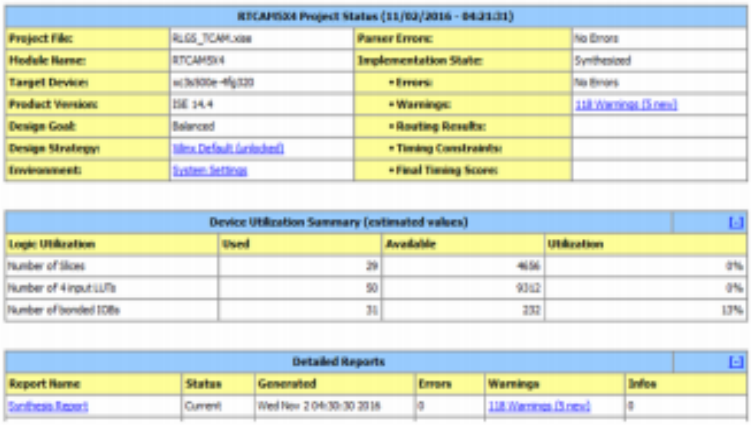

Fig.3. Summary Analysis

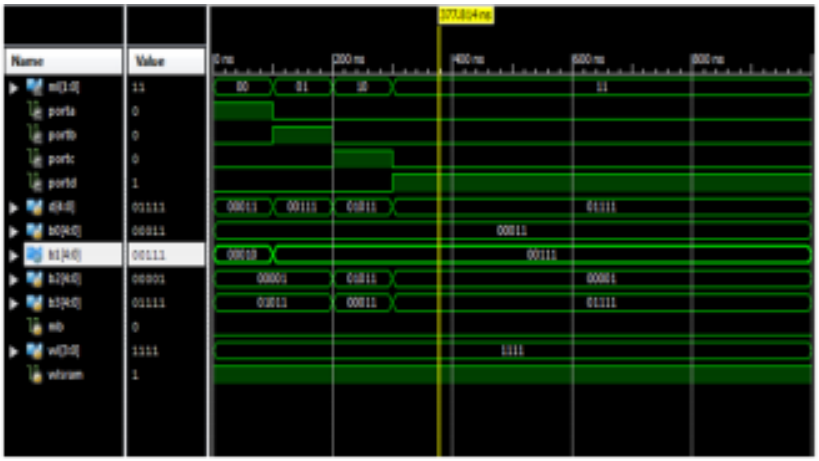

Fig.4. Simulation Analysis

Above two Designs perform the same operations which are verified on Xilinx ISE 14.7 simulator and compared the designs in terms of cost performance and garbage Outputs which varies slightly In above designs we have only tried to reduce the quantum cost and delay of the circuit and compare the both the design for single bit we can also design for array of cells and compare the results which is also done using Xilinx tool and verified on FPGA kit.

CONCLUSION

This paper proposed a novel design of TCAM design using reversible circuit design. Ternary content addressable memory compares input data against stored data (logic ’0’, logic ’1’, don’t care) in parallel and outputs the matched data. In reversible SRAM design, 3 × 3 Fredkin gate and the 2 × 2 Feynman gate is used to form the SRAM cell which is used to store the single bit of information. Each and every SRAM cell will have word line (WL) in order to make the SRAM cell to function in one of the modes that is either

in read/write or hold state. 3×3 Fredkin gate and Peres gate is used to perform the search line and match line operation. The design is verified and simulated by using Xilinx ISE simulator. The practical realization of reversible TCAM based chip will definitely reduce the power consumption of the network switches.

REFERENCES

1. Sk Noor Mahammad, Siva Kumar Sastry Hari,, " Constructing Online Testable Circuits Using Reversible Logic Reconfigurable and Intelligent Systems Engineering Group.
2. Kostas Pagiamtzis , Ali Sheikholeslami, "Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey", IEEE JOURNAL OF SOLID-STATE CIRCUITS VOL. 41, NO. 3, MARCH 2006
3. Vinay Kumar Gollapalli and K Koteshwarrao, M. Tech, SSGN Srinivas, M. Tech, "Design of Reversible Code Converters Using Verilog HDL",International journal and Magazine of Engineering technology management and Research, 2015.
4. Md. Selim Al Mamun, David Menville " Quantum Cost Optimization for Reversible Sequential Circuit" (IJACSA) International Journal of Advanced Computer Science and Applications, Vol. 4, No. 12, 2013.
5. Jagadeesh. D. Pujari, Rajesh. Yakkundimath and A. S. Byadgi, "Algorithm andArchitecture for a
6. Low-Power Content-Addressable Memory Basedon Sparse Clustered Networks ", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 23, NO. 4.