INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2442 - 2446
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

Design Low-Power and Area-Efficient Shift Register using SSASPL Pulsed Latch

[1]D. Sandhya Rani, [2]Maddana,

[1]PG Scholar, Dept of VLSI System Design, Geetanjali college of engineering & technology,
[2]Hod Dept of ECE, Geetanjali college of engineering & technology.

Abstract:

As the Word length of the shift register increases, the area and power consumption also increases. This paper proposes a low power and area efficient shift register by register reusing. In this system the multiple non-overlap delayed pulsed clock signals is used which timing problem between pulsed latches. The small number of pulsed clock signals used by grouping the latches to several subshift registers. Moreover, the similar functional operation of Register Reusing has been explained by using the Twisted Ring counter. .In digital circuits, a shift reg- ister is a cascade of flip flops, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input.More generally, a shift register may be multidimen- sional, such that its "data in" and stage outputs are them- selves bit arrays: this is implemented simply by running several shift registers of the same bit-length in parallel.

Keywords: Pulsed latches, pulsed Generator, Twisted Ring counter (TRC), Sub Shift Registers.

1. INTRODUCTION

A shift register is the basic building block in a VLSI cir- cuit. Shift registers are commonly used in many applica tions, such as digital filters, communication receivers and image processing ICs Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs.

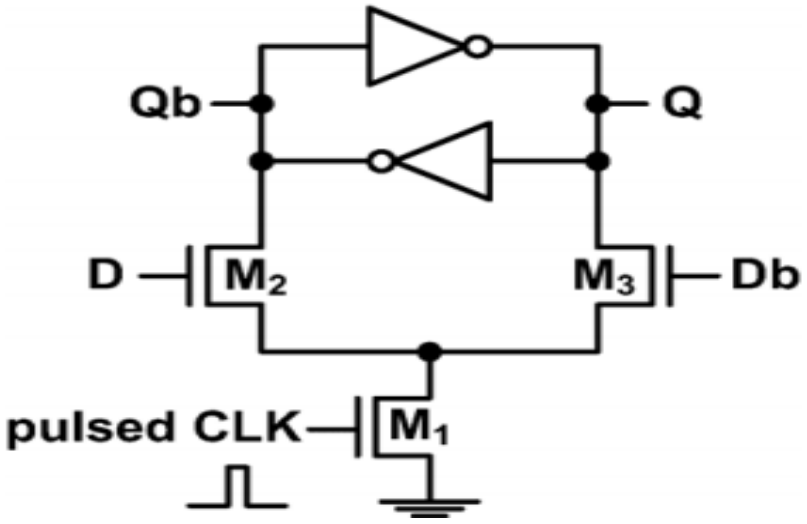

Fig.1. Schematic structure

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2442 - 2446
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register A 16- megapixel CMOS image sensor uses a 45K-bit shift regis- ter. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip- flops in many applications, because a pulsed latch is much smaller than a flip-flop [6]–[9]. But the pulsed latch can- not be used in a shift register due to the timing problem between pulsed latches. This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small num- ber of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional tempo- rary storage latches.Shift registers can have both parallel and serial inputs and outputs.

2. RELATED WORK

But real designs have a wide variation in clock and data activity across different TE instances. For example, low- power microprocessors make extensive use of clock gat- ing resulting in many TEs whose energy consumption is dominated by input data transitions rather than clock transitions. Other TEs, in contrast, have negligible data input activity but are clocked every cycle.

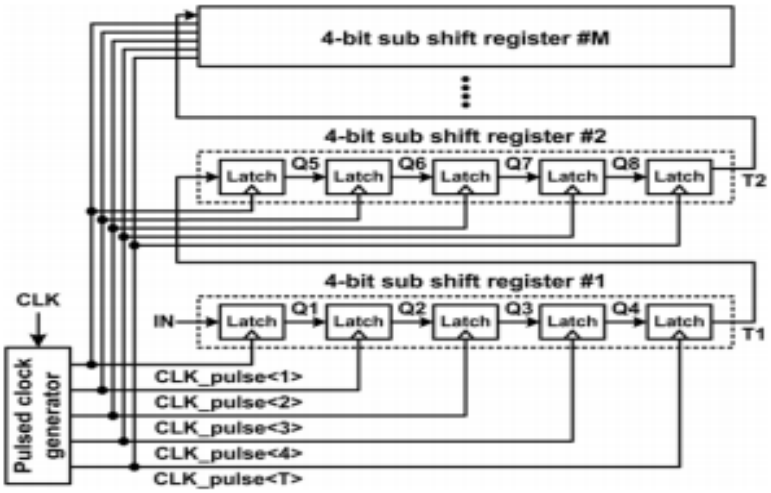

Fig.2.Proposed Structure

Shift registers, like counters, are a form of sequential logic. Sequential logic, unlike combinational logic is not only affected by the present inputs, but also, by the prior history. In other words, sequential logic remembers past events.Pulsed latch structures employ an edge-triggered pulse generator to provide a short transparency window. Com- pared to master–slave flip-flops, pulsed latches have the advantages of requiring only one latch stage per clock cycle and of allowing time-borrowing across cycle boundaries. The major disadvantages of pulsed latch structures are the increased susceptibility to timing hazards and the energy dissipation of the local clock pulse generators. Pulse generators can be shared among a few latch cells to reduce energy, if care is taken that the pulse shape does not degrade due to wire delay, signal coupling and noise. We measured designs both with individual pulse genera- tors and with pulse generators

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2442 - 2446
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

shared among four latch bits, in which case we divide the pulse generator energy among the four latch instances.

3. IMPLEMENTATION

Another solution is to use multiple non-overlap delayed pulsed clock signals. The de- layed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits. shows an example the proposed shift register. The pro- posed shift register is divided into M sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals. The number of clock buffers is K.

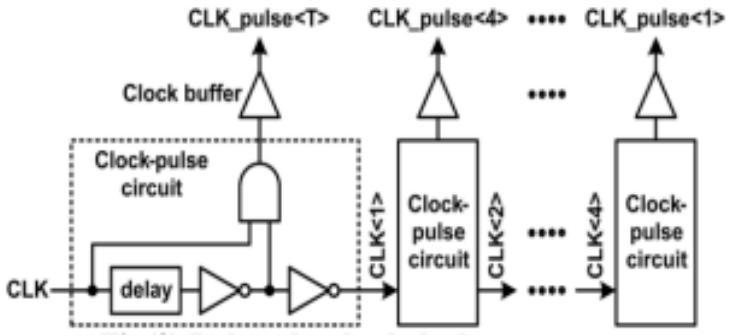

Fig.3.Clock Generator

As K increases, the size of a clock buffer decreases in pro- portion to 1/K because the number of latches connected to a clock buffer (M=N/K) is proportional to1/K. There- fore, the total size of the clock buffers increases slightly with increasing and the effect of the clock buffers can be neglected for choosing K.The maximum number of K is limited to the target clock frequency. As shown in Fig. 2.6 the minimum clock cycle time (TCLK-MIN) is TCP+K*TDELAY+TCQ, where TCP is the delay from the rising edge of the main clock signal (CLK) to the rising edge of the first pulsed clock signal decreases in proportion to 1/K. Therefore, K must be selected under the maximum number which is determined by the maximum clock frequency of the target applications.

4. ANALYSIS

The original SSASPL with 9 transistors is modified to the SSASPL by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transis- tors (7 transistors) and it consumes the lowest clock pow- er because it has a single transistor driven by the pulsed clock signal. The SSASPL was implemented and simulated with a 0.18µm CMOS process at VDD=1.8V. The sizes (W/L) of the three NMOS transistors (M1-M3) are 1µm/0.18µm. The sizes of the NMOS and PMOS transistors in the two inverters are all 0.5µm/0.18µm . The minimum clock pulse width of the SSASPL to update the data is 62 ps at a typical

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2442 - 2446
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

process simulation (TT) and 54–76 ps at all process corner simulations (FF-SS). A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches.

		Total number of transistors	Number of transistors connected to clock
Pulsed latch	**SSASPL [6]**	**7**	**1**
	TGPL [7]	10	4
	HLFF [8]	14	2
	CP3L [9]	26	6
Flip-flip	**PPCFF [10]**	**16**	**8**
	SAFF [11]	18	3
	DMFF [12]	22	5
	CPSA [13]	28	5
	CCFF [14]	28	5
	ACFF [15]	22	4

Fig.4. Performance Comparison

A 256-bit shift register was fabricated using a 0.18µm CMOS process with VDD=1.8V. Its core area is 6600µm2. It consumes 1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops.

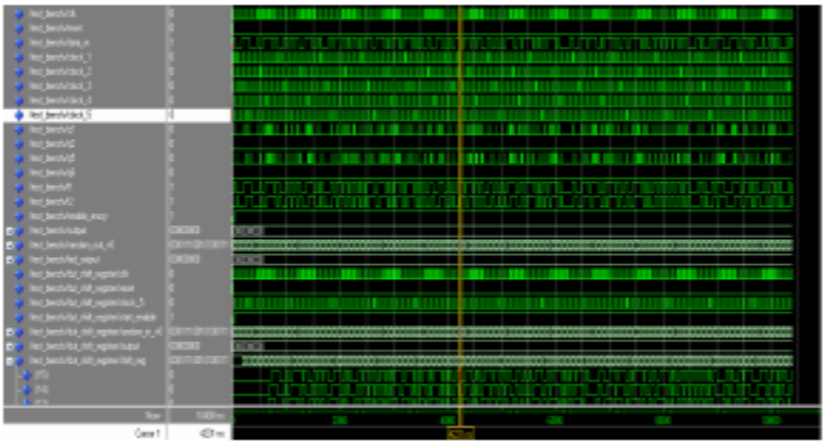

Fig.5.Output Wave

CONCLUSION

This paper proposed a low-power and area-efficient shift register using digital pulsed latches. The shift register reduces area and power consumption by replacing flip- flops with pulsed latches.The timing problem between pulsed latches is solved using multiple non-overlap de- layed pulsed clock signals instead of a single pulsed clock signal.

REFERENCES

[1] P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, “New protection techniques against SEUs for moving average filters in a radiation environment,” IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 957–964, Aug. 2007.

[2] M. Hatamian et al., "Design considerations for giga- bit ethernet 1000 base-T twisted pair transceivers," Proc. IEEE Custom Integr. Circuits Conf., pp. 335–342, 1998.
[3] H. Yamasaki and T. Shibata, "A real-time image- feature-extraction andvector-generation vlsi employing arrayed-shift-register architecture," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 2046–2053, Sep. 2007.
[4] H.-S. Kim, J.-H. Yang, S.-H. Park, S.-T. Ryu, and G.-H. Cho, "A 10-bitcolumn-driver IC with parasitic-insensitive iterative charge-sharing based capacitor-string interpola- tion for mobile active-matrix LCDs," IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 766–782, Mar. 2014.
[5] S.-H. W. Chiang and S. Kleinfelder, "Scaling and de- sign of a 16-megapixelCMOS image sensor for electron microscopy," in Proc. IEEE Nucl. Sci. Symp. Conf. Re- cord (NSS/MIC), 2009, pp. 1249–1256.
[6] S. Heo, R. Krashinsky, and K. Asanovic, "Activity- sensitive flip-flopand latch selection for reduced energy," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 9, pp. 1060–1064, Sep. 2007.