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# Pass Transistor and CMOS Logic Configuration based De-Multiplexers

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**Abstract**:

Pass Transistor Logic (PTL) configuration describes several logic families used in the design of integrated circuits. It reduces the count of transistors used in making different logic gates, by eliminating redundant transistors. The pass transistor is driven by a periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance, depending on the input signal. CMOS logic is easy to design but very resource consuming. Comparisons between the efficacies of both the logics are analyzed by implementing 1:2 De-Multiplexer using two configurations. Besides this, decrement in power dissipation up to 70% is achieved in pass transistor logic.

**Keywords:** PTL, CMOS Logic, De-Multiplexer.

## 1. INTRODUCTION

VLSI is dominated by the CMOS technology and much like other logic families, this too has its limitations which have been battled and improved upon since years. As the number of transistors increase, the power dissipation is increasing and also the noise. If heat generated per unit area is to be considered, the chips have already neared that of the nozzle of a jet engine.

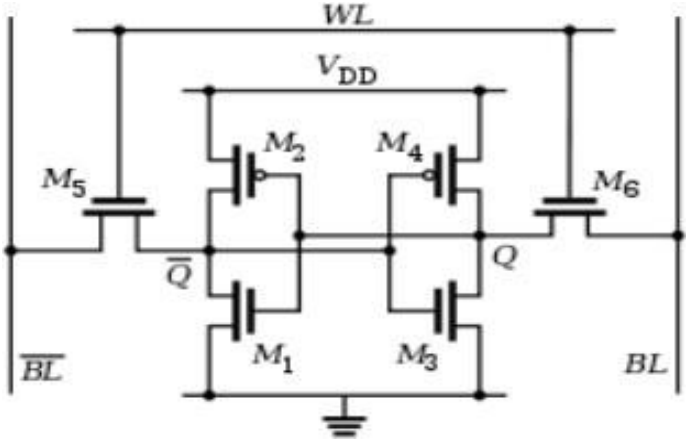


**Fig.1.General Structure**

Pass Transistor Logic describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly

to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.

## 2. RELATED WORK

As Some authors use the term "complementary pass transistor logic" to indicate a style of implementing logic gates that uses transmission gates composed of both NMOS and PMOS pass transistors. Other authors use the term "complementary pass transistor logic" (CPL) to indicate a style of implementing logic gates where each gate consists of a NMOS pass transistor network, followed by a CMOS output inverter. Some use the term "complementary pass transistor logic" to indicate a style of implementing logic gates using dual-rail encoding. Every CPL gate has two output wires, both the positive signal and the complementary signal, eliminating the need for inverter six-transistor CMOS SRAM cell. From Fig: 1 M5 and M6 are bidirectional pass transistors. The data distributor, known more commonly as a Demultiplexer or "Demux" for short, is the exact opposite of the Multiplexer. The demultiplexer takes one single input data line and then switches it to any one of a number of individual output lines one at a time. CMOS logic architecture is one of the most commonly used logic configuration employed in digital circuit designing but it has its own merits and demerits. Few are described here such as large numbers of transistors are required even to implement simple circuits like basic logic gates and inverter circuit depicts CMOS architecture of 1:2 de- multiplexers. It is clear from the diagram that 14 transistors are required to implement this device. Six transistors for each AND gate and two for NOT gate, where S is selection line. The IN is input that is applied to both the AND gates. OUT1 and OUT2 represent output lines. The selection of these lines is dependent on terminal S. It can also be understood from the figure that large number of interconnects are used in this approach to connect numerous transistors. Therefore, CMOS logic is easy to design but very resource consuming.

## 3. PROPOSED SYSTEM

The implementation of 1:2 de-multiplexers using pass transistor logic configurations require only six transistors to implement the complete logic architecture. This means that number of transistors used in pass transistor architecture is less than that of the transistors utilized in CMOS architecture. Therefore, it is evident from the facts stated show that the area consumption is 50% less using pass transistor logic architecture. Moreover, lesser interconnect lengths and fewer transistors allows a decrement in fabrication cost too. Moreover, the fabrication steps and resources are also decreased/ consumed less in pass transistor logic implementation. Therefore, results observed in both the architecture is stated that pass transistor architecture is more area efficient than ordinary CMOS architecture. The comparison between CMOS and pass transistor logic architectures are discussed in this section. Besides this, analysis also done to identified the better driving capability among both the architectures. Output current levels of CMOS and pass transistor logic architecture are shown respectively. These characteristic plots are of the output current level of CMOS logic and pass transistor logic circuits that determine their driving capability. Results indicated

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that pass transistor logic configuration is the better options used in high speed and compact digital circuitry Pavg of the transistor. Any change in supply voltage is directly reflected on to the power dissipation. It is observed and power dissipation for similar output current.

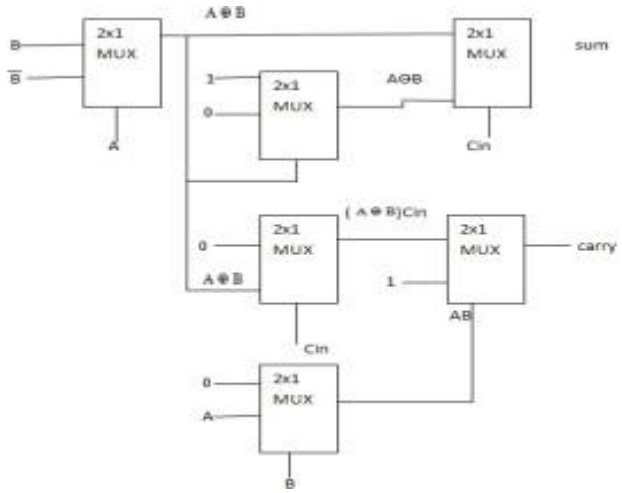


**Fig.2.Block Diagram**

By Ohm‟s law, if by reducing the supply voltage from 1.8V to 1.2V for pass transistor logic architecture, It gets the maximum output current level of the architecture around 35μA i.e. almost similar to the maximum output current level of CMOS architecture. Now power dissipation can be compared of the architectures as both are having similar output current level.

## 4. ANALYSIS

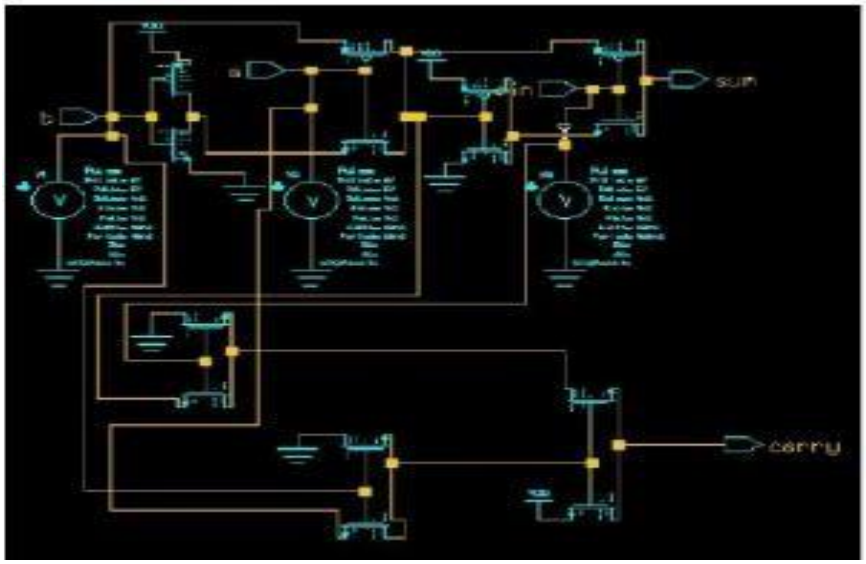


**Fig.3.Struture design**

 

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Where αTi is corresponding node transition factor, Ci is parasitic capacitance associated with each node, Vi is node voltage, VDD is supply voltage and Fclk is clock frequency. It is prominent from the equation that number of operating nodes also contribute to the overall power dissipation of the device. Since CMOS logic implementation requires larger number of transistors therefore operating points is higher in CMOS logic implementation than pass transistor logic implementation. Another important point i.e. supply voltage of pass transistor logic architecture.

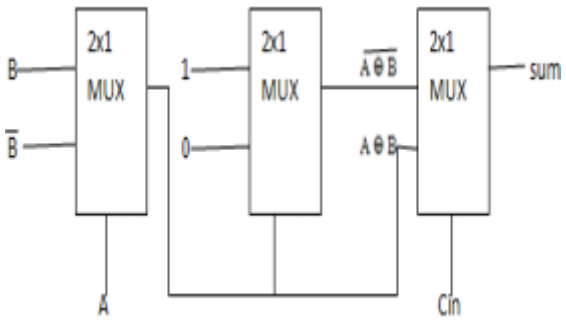


**Fig.4.Demultiplexer output**

It is reduced by 33% (0.6V) making it further power efficient. In the proposed paper we are concentrating mainly on full adder implementation as it finds use in many of the low power applications. A basic full adder can be implemented with XOR gate, AND gates and OR gate. The logic for sum can be realized using XOR gate whereas the logic for carry can be realized using AND and OR gates. It shows that the entire full adder logic is based on its sum and carry outputs. Reducing the transistor counts in sum and carry logic may reduce the size of the full adder. For that purpose a mixed CMOS based full adder circuit is proposed in the present paper In the proposed paper we are concentrating mainly on full adder implementation as it finds use in many of the low power applications. A basic full adder can be implemented with XOR gate, AND gates and OR gate. The logic for sum can be realized using XOR gate whereas the logic for carry can be realized using AND and OR gates. It shows that the entire full adder logic is based on its sum and carry outputs. Reducing the transistor counts in sum and carry logic may reduce the size of the full adder. For that purpose a mixed CMOS based full adder.

## CONCLUSION

This paper analyzed the performance of 1:2 De- Multiplexer using Pass Transistor Logic and CMOS Logic. The results observed that approximately 50% of chip area is saved by using the pass transistor logic configuration as only six transistors (6-T) are employed to implement the 1:2 De-multiplexer while fourteen transistors (14-T) are used in CMOS logic architecture. The power supply is reduced by 33% observed due to processes with pass transistor logic. Moreover, 70% reduction in power dissipation is analyzed with pass transistor. Therefore, it can be concluded that the pass transistor logic implementation of 1:2 de-multiplexer gives better performance and consumes less chip area in comparison to CMOS logic architecture.

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