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Realization of programmable logic array using compact reversible logic gates

[1]E. Chandini, [2]Shankarnath, [3]Madanna ,

[1]PG Scholar, Dept of VLSI System Design, Geethanjali college of engineering and technology,
[2]Assistant professor, Dept of ECE, Geethanjali college of engineering and technology,
[3]HOD Dept of ECE, Geethanjali college of engineering and technology.

Abstract:

A Decoder circuit converts a binary integer value to an associated pattern of output bits. They are used in various applications like data de-multiplexing, seven segment display, and memory address decoding. Day by day as the technology is advancing systems are becoming more compact. Power dissipation plays a critical role in design of low power circuit. Reversible logic has become the most promising technology in designing digital circuits. The research on reversibility has shown greater impact to have many applications in emerging technologies such as Quantum Computing, QCA, Nanotechnology and Low power VLSI. In this paper we have proposed designs of 2:4 decoder using reversible logic gates. The gate simulations of the proposed decoder are shown using QUARTUS II 9.1 Modelsim, which proved the functional correctness of the proposed circuits.

Keywords: Reversible Logic, Reversible Decoder, NFT Gate, RI Gate.

1. INTRODUCTION

With the advancement in technology, the device dimensions are shrinking exponentially and so the circuit complexity is growing exponentially. After certain point the device scaling is restricted due to power dissipation, which has created curiosity in research area of Reversible Logic circuits. According to Rolf Landauer [1], heat generated due to the loss of one bit of information during computation is about KTln2 in joules where K is the Boltzmann constant and T is the absolute temperature at which computation is performed. Bennett proposed a solution to the problem of heat dissipation. Bennetee [2] showed in order to avoid kT*ln (2) joules of energy dissipation in a circuit it must be built from reversible circuits. Reversible circuit do not lose information. A circuit will be reversible if input vector can be specifically retrieved from output vectors and here is one to one correspondence between input and output [3]. Reversible logic gates have same number of input and outputs, since in reversible circuits no bit loss is there hence ideally in reversible circuits no power dissipation occurs. But practically some power dissipation does occur, which is much less than the conventional logic. The extra output used in order to make inputs and outputs equal are called garbage outputs. The circuit should be designed in such a manner so as to keep these outputs minimum. However, in certain reversible circuits constant inputs are also used. These constant inputs are set either to logic 1 or logic 0 depending upon the operation of the circuit.

2. RELATED WORK

The internal architecture of CPU consisting of Control Unit, ALU, Register files and various components which plays an important role in performance of whole CPU. Control Unit directs the operation within the computer processor by directing the inputs and outputs of computer system. Important block of

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control unit is decoder, which is used to control the memory components of processor plays an extensively important role in performance of overall CPU. Hence it will be not wrong if we say the instruction set decoder consumes more power. Thus optimizing the power of this block will be helpful to reduce the overall power consumption of the system. Md. Shamsujjoha and Hasan Babu proposed a fault tolerant reversible decoder [4,5] [5, 6] in 2013. Only a F2G can work as 1-to-2 Reversible Fault Tolerant Decoder (RFD) can be used in parallel circuits, multiple-symbol differential detection, network components and in digital signal processing etc.

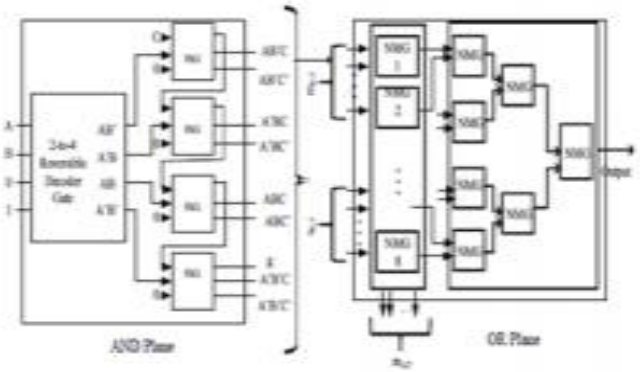

Fig.1. Part of proportion

A 2-to-4 reversible fault tolerant decoder can be realized with at least 12-quantum cost using one F2G and 2 FRG and further a 3-to-8 reversible fault tolerant decoder design requires six Fredkin gates and one Feynman double gate. The constructed circuit can detect any single bit errors that include single bit stuck-at-fault. An advantage is that the technique ensures that the garbage generated during the process of conversion to testable reversible circuit is minimized. HV, Et al. in year 2012 designs the 2:4 Decoder, which requires 1 Feynman and 2 Fredkin Gates. This design requires a total of 3 gates with constant input 3 and garbage output as 1. This design requires a total of 3 gates, number of inputs is 5, which include 2 variable inputs and 3 constant inputs, garbage output 1, delay of 1 and quantum cost 11. This work in terms of performance is quite effective but the design algorithm has not been extended for further 3:8 and 4:16 decoder. Arvind Kumar, Et al. concluded that the 2 to 4 decoder using three fredkin gates. Since in all three Fredkin gates same number of inputs and outputs resulting in less power dissipation as compared to conventional logic gates. Hence by making use of fredkin gates in similar manner any n to 2n decoder can be designed.

3. IMPLEMENTATION

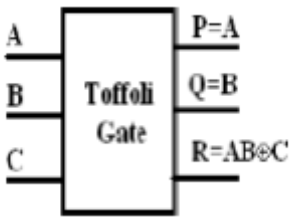

Fig.2. Gate model

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In Design 1 suing NFT gate we have used 2 NFT gates and 2 NOT gates. As NOT gates quantum cost is zero the Quantum cost of 2:4 Decoder is 10. One constant input to each of the NFT is given as zero and it generated 2 Garbage output. Fig.6 shows 2:4 Decoder using NFT and NOT gate. Here input A to both the NFT gate is given as zero, which results in output of first NFT as BC', BC and second NFT as B'C, B'C'. Number of Gates used in 2:4 Decoder Design 1 and 2 are same but the Quantum cost of Design 2 is less compared to Design 1. Implementation of 3:8 Decoder using Design 2 is shown in Fig.9 As see output of 2:4 Decoder is given further to 4 different R-I Gate which generated required output for 3:8 Decoder. As observed the number of Garbage outputs are less because output from one R-I gates is given as input to other. The design utilizes in total 6 R-I gates and 2 NOT gate. The Quantum cost of the 3:8 decoder using R-I gate is 24.

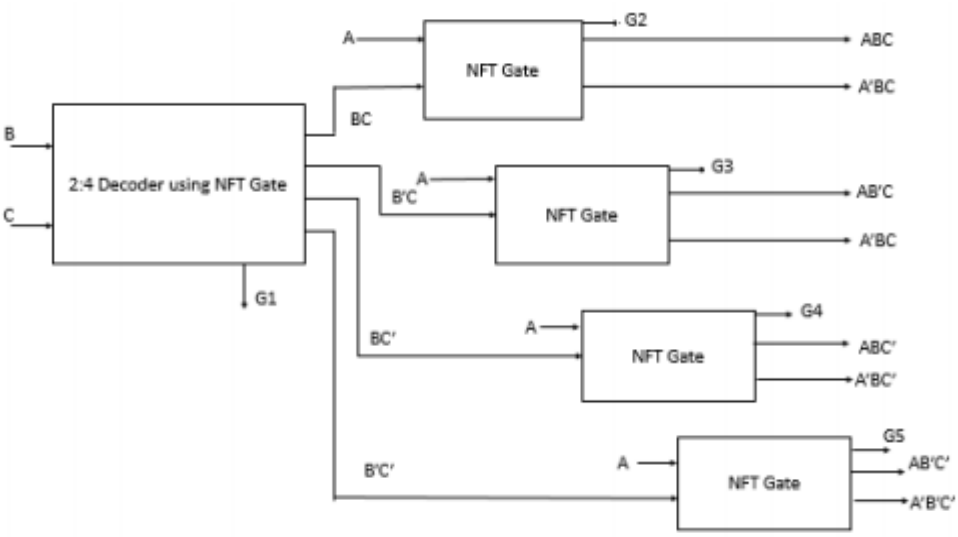

Fig.3. Proposed model

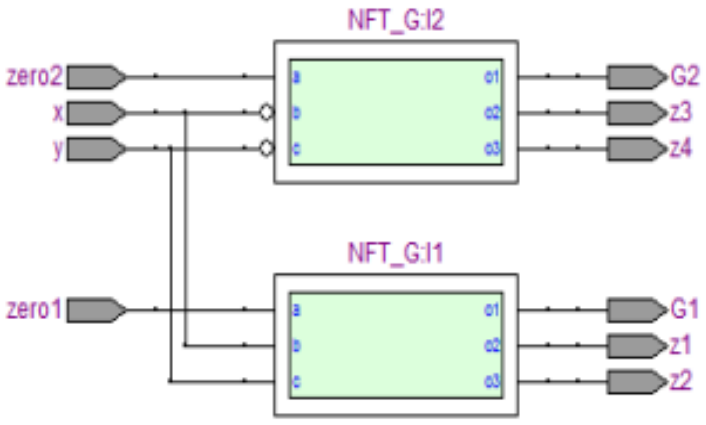

Fig.4. Decoder NFT gate

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4. ANALYSIS

A 3-input RPLA circuit using Feyman and Fredkin (FRG) gate is designed in [4]. Total 16 FRG gates are used to generate minterms of 3variables,lettingfirst two outputs of all FRG gates as don't care outputs which cause huge garbage outputs. This design is not programmable. That is, the designers cannot program its array to generate any desirable function. Authors in [5] showed a cost effective method to design the RPLA with MUX gate instead of FRG gate. It also has problem in scalability and dynamism. Authors in [6] proposed 4 different architectures of AND plane.

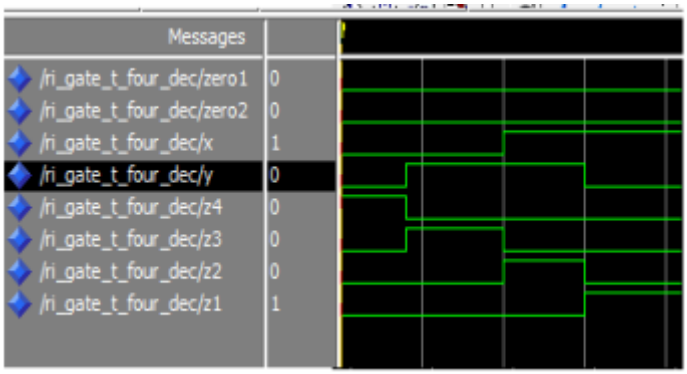

Fig.5. Simulation

All the existing designs require huge constant inputs and gate, produce extra garbage outputs and have high quantum cost. In this paper, we propose a compact and low cost architecture of RPLA circuit. And finally, the NMG gate of the last column produces the main output O of the OR array which is the OR of all mi.si's, for i = 0 to 7. The main output of this OR array, O, can be programmed through the selector lines, si, to produce any desired boolean function. The selector lines can be changed to set or reset to select the appropriate minterms of a function. The proposed design of the OR array also produces a copy of the minterms at its outputs. These minterms can be used in another OR array to produce another Boolean function, without need to use another AND array.

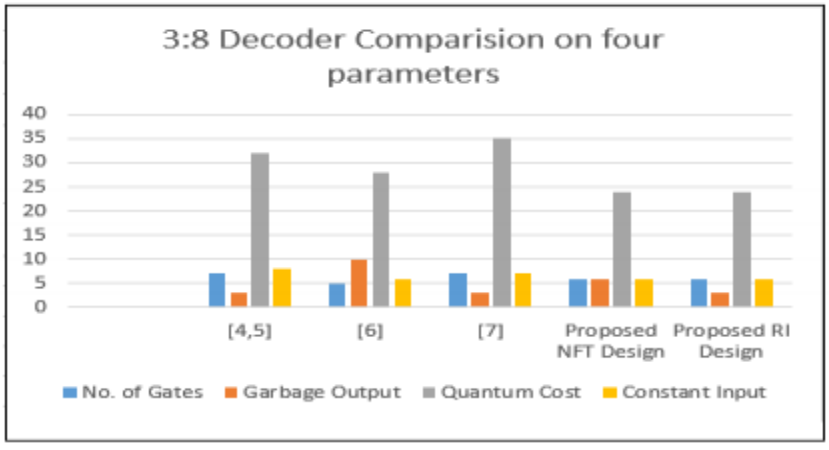

Fig.6. Graph analysis

CONCLUSION

In this paper an optimized 2:4 and 3:8 Decoder designs with two different approach is proposed. The proposed designs are being implemented using VHDL in Quartus II 9.1 and simulation waveform for the Decoders (using Quartus II 9. Modelsim) are shown. The proposed designs are compared with the existing designs and the comparison study is shown. The proposed design with R-I gate gives better results in terms of number of Garbage outputs generated and the Quantum cost.

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