INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2417 - 2421
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

A Compact Design of 8X8 Bit Vedic Multiplier Using Reversible Logic Based Compressor

[1]Viswanath Gowthami, [2]B.Govardhana, [3]Madanna ,

[1]PG Scholar, Dept of VLSI System Design, Geethanajali college of engineering and technology,
[2]Assistant professor Dept of ECE, Geethanajali college of engineering and technology,
[3]HOD Dept of ECE, Geethanajali college of engineering and technology.

Abstract:
Reversible logic gates became very important and computing paradigm having its applications in low power CMOS technologies and Quantum computing we proposed reversible gates methodology also introduces for quantum cost reducing of circuit. With the advent of new technology in the fields of VLSI and communication, there is also an ever growing demand for high speed processing and low area design. It is also a well-known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. In this paper, we introduce a novel architecture to perform high speed multiplication using ancient Vedic math techniques. A new high speed approach utilizing 4:2 compressors and novel 7:2 compressors for addition has also been incorporated in the same and has been explored. Upon comparison, the compressor based multiplier introduced in this paper, is almost two times faster than the popular methods of multiplication. The design and experiments were carried out on a Xilinx and the timing and area of the design, on the same have been calculated.

Keywords: Reversible Gates, Compressors, Vedic Multiplier.

1. INTRODUCTION

The speed of a processor greatly depends on its multiplier‟s performance. This in turn increases the demand for high speed multipliers, at the same time keeping in mind low area and moderate power consumption. Over the past few decades, several new architectures of multipliers have been designed and explored. Multipliers based on the Booth‟s and modified Booth‟s algorithm is quite popular in modern VLSI design but come along with their own set of disadvantages. In these algorithms, the multiplication process, involves several intermediate operations before arriving at the final answer.

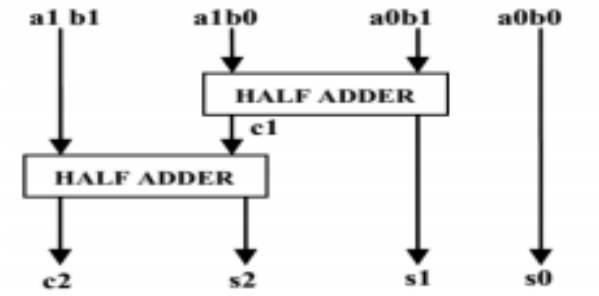

Fig.1. Basic Structure

The intermediate stages include several comparisons, additions and subtractions which reduce the speed exponentially with the total number of bits present in the multiplier and the multiplicand. Since speed is our major concern, utilizing such type of architectures is not a feasible approach since it involves several

time consuming operations. In order to address the disadvantages with respect to speed of the above mentioned methods, and explored a new approach to multiplier design based on ancient Vedic Mathematics. Vedic Mathematics is an ancient and eminent approach which acts as a foundation to solve several mathematical challenges encountered in the current day scenario. Vedic Mathematics existed in ancient India and was rediscovered by a popular mathematician, Sri Bharati Krishna Tirthaji. He bifurcated Vedic mathematics into 16 simple sutras (formulae). These Sutras deal with Arithmetic, Algebra, Geometry, Trigonometry, Analytical Geometry etc. In this paper, we explore a novel method to further enhance the speed of a Vedic mathematics multiplier by replacing the existing full adders and half adders of the Vedic mathematics based multipliers with compressors by using Compressors, in its several variants, are logic circuits which are capable of adding more than 3 bits at a time as opposed to a full adder and capable of performing this with a lesser gate count and higher speed in comparison with an equivalent full adder circuit.

2. RELATED WORK

The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The Net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies.By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures.

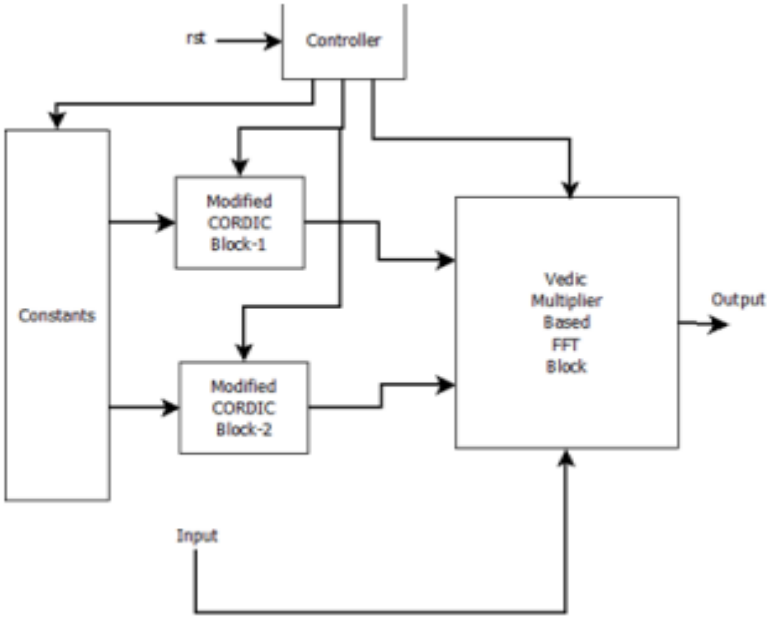

Fig.2. Process controller

The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed. In conventional method, partial products are summated only after every partial product is obtained. Whereas, in Vedic technique,

INTERNATIONAL RESEARCH JOURNAL IN ADVANCED ENGINEERING AND TECHNOLOGY (IRJAET) E - ISSN: 2454-4752 P - ISSN : 2454-4744
VOL 3 ISSUE 6 (2017) PAGES 2417 - 2421
RECEIVED : 25.10.2017 PUBLISHED : 13.11.2017
Nov 13, 2017

partial products are obtained vertically as shown in the figure above and simultaneously once all the elements of a column are obtained, respective partial products are added. Hence, leads to advancement in speed over the conventional method.

3. IMPLEMENTATION

The architecture is connected in such a way that four of the inputs are coming from the same bit position of the weight j while one bit is fed from the neighboring position j-1(known as carry-in). The outputs of 4:2 compressors consist of one bit in the position j and two bits in the position j+1. This structure is called compressor since it compresses four partial products into two (while using one bit laterally connected between adjacent 4:2 compressors). An alternative implementation is shown in Fig.5. This implementation is better and involves a critical path delay of three XOR‟s, hence reducing the critical path delay by 1 XOR. The output C out, being independent of the input C in accelerates the carry save summation of the partial products. Compressors are used to implement arithmetic and digital signal processing architectures for high performance applications.

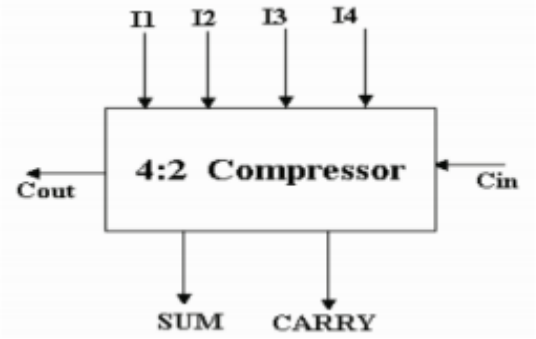

Fig.3. Compressor system

These are used especially in adder structures to reduce the complexity and time delay. These are also used in Multiplier architectures to add all partial products and for final addition. In multiplier architectures the main source of power, delay and area consumption are from how these partial products are accumulated. These compressors are used to reduce time delay and increase its speed for specific architecture. Generally compressors reduce N-input bits to a single sum bit of equal weight to that of the inputs and carry out bit. In usage we had 3:2, 4:2, 5:2, etc. In this paper we used only 4:2 compressors with four inputs (x1, x2, x3, x4) and two outputs sum and carry. The 4:2 compressors receive an input Cin from the preceding module of one binary bit order lower in significance, and produce an output Coutto the next compressor module of higher significance as shown in figure . Besides, to accelerate the carry save summation of the partial products, it is imperative that the output, Coutbe independent of the input Cin. Figure a describes an 4 input TSG reversible logic gate with 4 outputs as shown above and by making input C as „0‟ it acts as Full Adder.

4. ANALYSIS

To generate Partial Products we used peres gates because quantum cost per gate is less when compared to other reversible gates. In literatureto generate partial products they used Fredkin gates or Peres gates. Quantum Cost for Fredkin gate is 5 but for Peres gate it is 4. So we choosen Peres gate to reduce QC. We require 64 gates to generate 64 partial products and the same This paper combines two different

technologies like Compressor logics and Reversible Logics for adding Partial Products on Vedic Multiplier and it was observed that number of stages and number of gates used reduces when compared to other existing structures.

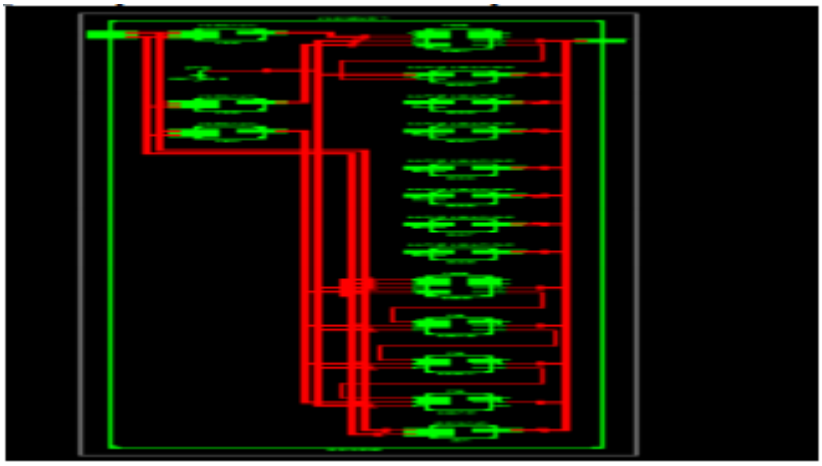

Fig.4. Analysis wave

The FFT module implementation is done using equation where Sinθ and Cosθ are generated for predefined angles of N point FFT. The proposed FFT uses modified CORDIC to generate twiddle factors for predefined angles and observed that it avoids ROM based storage and Look Up Table method of storage. This results in high speed operation of FFT block with less hardware. The multiplications present in FFT are replaced by Vedic multiplier to increase frequency.

CONCLUSION

Compressor based Vedic Multiplier has been designed using Reversible logics and the functional correctness of the proposed Vedic multiplier. We have proposed a novel high speed architecture for multiplication of two 8 bit numbers, combining the advantages of compressor based reverse logic adders and also the ancient Vedic math‟s methodology. A new 4:2 compressor designed with reversible gates architecture was also discussed. Upon comparison of the area occupied by the multiplier and also its speed, with two other popular multipliers. we can conclude that the compressor based reverse Vedic math‟s multiplier proves to be a better option over conventional multipliers used in several expeditious and complex VLSI circuits.

REFERENCES

[1]D. Radhakrishnan A.P. PreethySingapore “Low Power CMOS Pass Logic 4-2 Compressor for High-Speed Multiplication”, circuits and systems, 2000, Proceedings of the 43rd IEEE Midwest Symposium, pages 1296-1298.

[2]S. F. Hsiao, M.R. Jiang and J.S. Yeh, "Design of high- speed low-power 3-2 counter and 4-2 compressor for fast multipliers," Electronics Letters, vol. 34, no. 4, pp. 341-342, Feb. 1998

[3]M.Margala and N.G. Durdle, "Low-Power Low-Voltage 4-2 Compressors for VLSI Applications," Proc. Workshop on Low Power Design, 1999.

[4]S.Veeramachanemi, K.Krishna, L.Avinash, S.R.Puppola, M.B.Srinivas, "Novel architectures for high speed and low power 3-2, 4-2 and 5-2 compressors", IEEE Proc .Of VLSID‟07,pp.324- 329,2007.

[5]HimanshuThapliyal and M.B Srinivas "Novel Reversible Multiplier Architecture Using Reversible TSG Gate" Computer Systems & Applications, 2006 IEEE International Conference, pages 100-103.

[6]Md. M. H Azad Khan, "Design of Full-adder With Reversible Gates", International Conference on Computer and Information Technology, Dhaka, Bangladesh, 2002, pp. 515-519.