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Design of low power, high performance 2-4 and 4-16 mixed logic line decoders

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Abstract:

In this paper, a 2-to-4 Decoder has been designed to reduce power consumption and surface area using 65nm, 45nm and 32nm complementary- metal- oxide- semiconductor technology, which is then analyzed and comparative study has been done in account of the silicon surface area and power consumption. The proposed 2-to-4 Decoder using 32nm CMOS technology gives better results in terms of power and surface area as compare to 45nm and 65nm COMS technologies. The 2- to-4 decoder circuit size is 14.3 µm2 and typical power consumption is 0.172 µW at 32nm CMOS technology. All simulation result and analysis are performing on 65nm, 45nm and 32nm complementary-metal-oxide- semiconductor technology, using DSCH and MICROWIND tools.

Keywords: CMOS, VLSI, 2-to-4 Decoder, Power consumption, CMOS technology.

1. INTRODUCTION:

In present scenario, power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. The chip density and higher operating speed leads to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products [2].

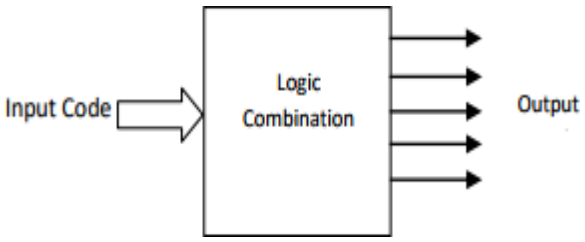

Fig.1. Basic Structure

The development of electronic technology was started with the use of vacuum tube as active component in electronic series before semiconductor transistor replaces it. The development of microelectronic technology especially for those of mono-litical is able to produce interfaced circuit by combining all active and passive components in one chip [3]. High speed serializer/deserializers (SerDes) are now more and more widely used in communication systems for serial interconnections [4]. Decoders are used whenever an output or a group of outputs is to activated only on the occurrence of specific combination of input levels.

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These input levels are often provided by the outputs of a counter or register. When the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially, and they can be used as timing or sequencing the signals to turn devices ON or OFF at specific times. Decoders are widely used in memory systems of computers, where they respond to the address code input from the central processor to activate the memory storage location specified by the address code [1].

2. RELATED WORK

In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs. The decoder identifies or recognizes or detects a particular code.

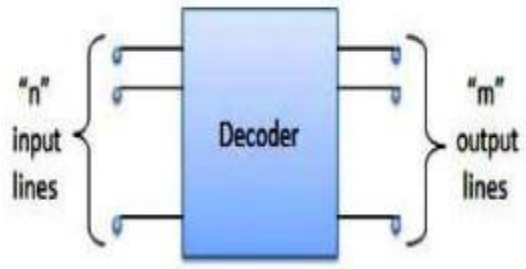

Fig.2. Block diagram

The N inputs can be a 0 or a 1, there are 2N possible input combinations or codes. For each of input combination only one of the M. Low power consumption has been a priority and so pass transistor based tree decoders have been selected due to the lower leakage and dynamic switching currents. An asynchronous design would further help to reduce the dynamic power dissipation from the clock switching. Reliability has been the second important priority and design procedures for high read and write margins tolerant to process variations have been developed [5]. The layout design of the basic layout is the general concept that describes the geometrical representation of the circuits by the means of layers. Different logical layers is used by designers to generate the layout.

3. IMPLEMENTATION

In this section, performance analysis of decoder has been presented. Designs simulations are done using DSCH and MICROWIND tools at different foundries like 65nm, 45nm, 32nm. Packing and particular manufacturing process including every small features have been described through the layout design rule. The designers have used different logic layers for layout generation. There are specific layers for metal, contacts or diffusion areas, polysilicon. Design red color presents polysilicon, green color indicates n+ diffusion, light green color indicates p+ diffusion, light and dark blue color within the layout designed. quently the heat generation is formidable. Bennett later showed that this heat dissipation can be avoided by using reversible computation. This proof by Bennett has led to an extensive research on reversible logic theory. The most prominent applications of these logics are seen in quantum computation, DNA computing, nanotechnology and low power CMOS design. Quantum logic gates are used to compose Quantum Networks- each gate performing an elementary unitary operation on one, two or more than two state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to

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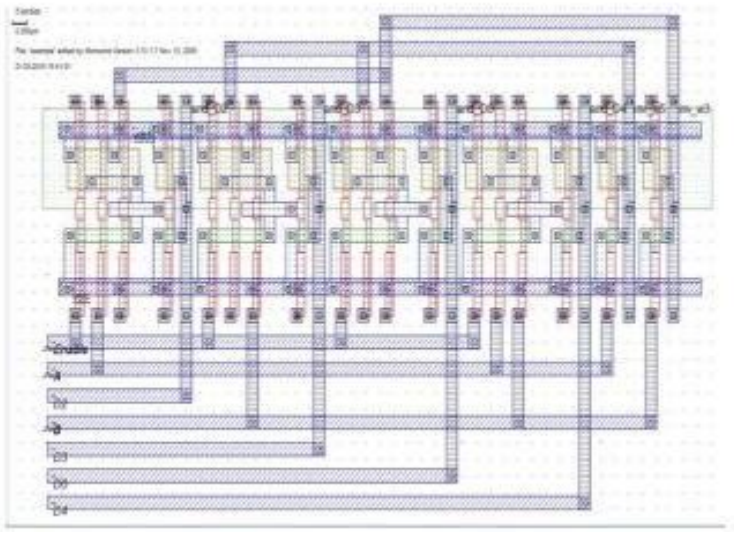

Fig. 3. Layout structure

the classical bit values 0 and 1. arithmetic must be built from reversible logic components. Quantum cost, delay, number of constant inputs and garbage outputs are the most important cost metrics of reversible computing [3] . The outputs which are present only to maintain reversibility and do not perform any useful operations are called as Garbage outputs. Number of gates is not a good measure of cost, since more than one gates can be taken together to form a new gate, thus reducing the gate count. Vanshikha Singh and Rajesh Mehra [5] stated the DA formulation employed for two separate blocks weight update block and filtering operations they demonstrated that the area is reduced in the full custom design of the decoder circuit from standard cell layout and the semi custom based layout of the decoder. The power is reduced in the semi custom design from standard cell layout but increased in the full custom design.

4. ANALYSIS

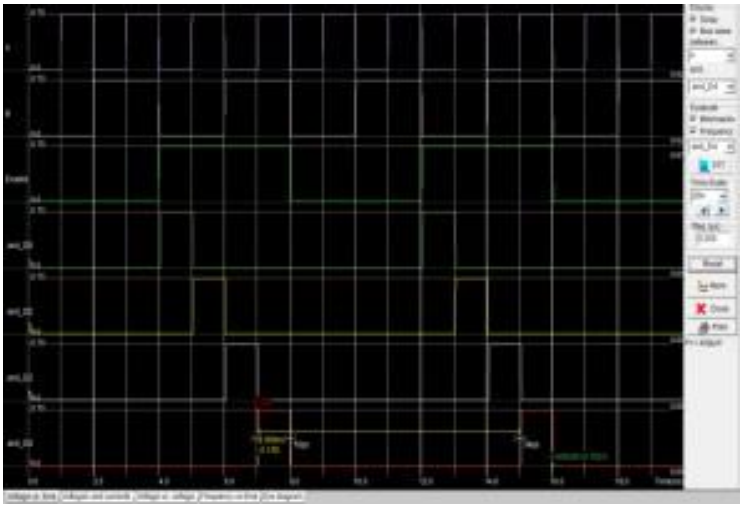

Fig.4. Wave analysis

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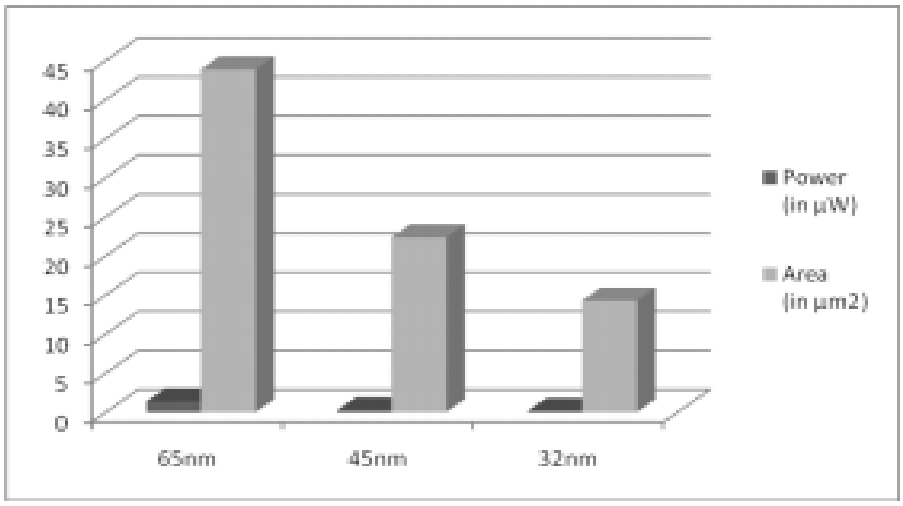

Fig.5. Analysis wave

In this section, performance analysis of decoder has been presented. Designs simulations are done using DSCH and MICROWIND tools at different foundries like 65nm, 45nm, 32nm. Packing and particular manufacturing process including every small features have been described through the layout design rule. The designers have used different logic layers for layout generation. There are specific layers for metal, contacts or diffusion areas, polysilicon. Design red color presents polysilicon, green color indicates n+ diffusion, light green color indicates p+ diffusion, light and dark blue color within the layout designed.

CONCLUSION

The proposed 2-to-4 Decoder is designed and simulated using 32nm, 45nm and 65nm CMOS technologies .The performance parameters power and surface area are examined. Low power consumption andefficient surface area is obtained using proposed logic for designed 2-to-4 Decoder. The power consumed by the circuit in 65nm, 45nm and 32nm CMOS technologies are 1.400 µW, 0.275 µW and 0.172 µW respectively. The surface area required for the circuit in 65nm, 45nm and 32nm CMOS technologies are 43.9 µm2, 22.4 µm2, and 14.3 µm2 respectively.

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